LCFC Confidential

VIENNA M/B Schematics Document

INTEL Bay Trail-M Platform

2013-10-22

REV:1.0

Security Classification	LC Future Center Secret Data		
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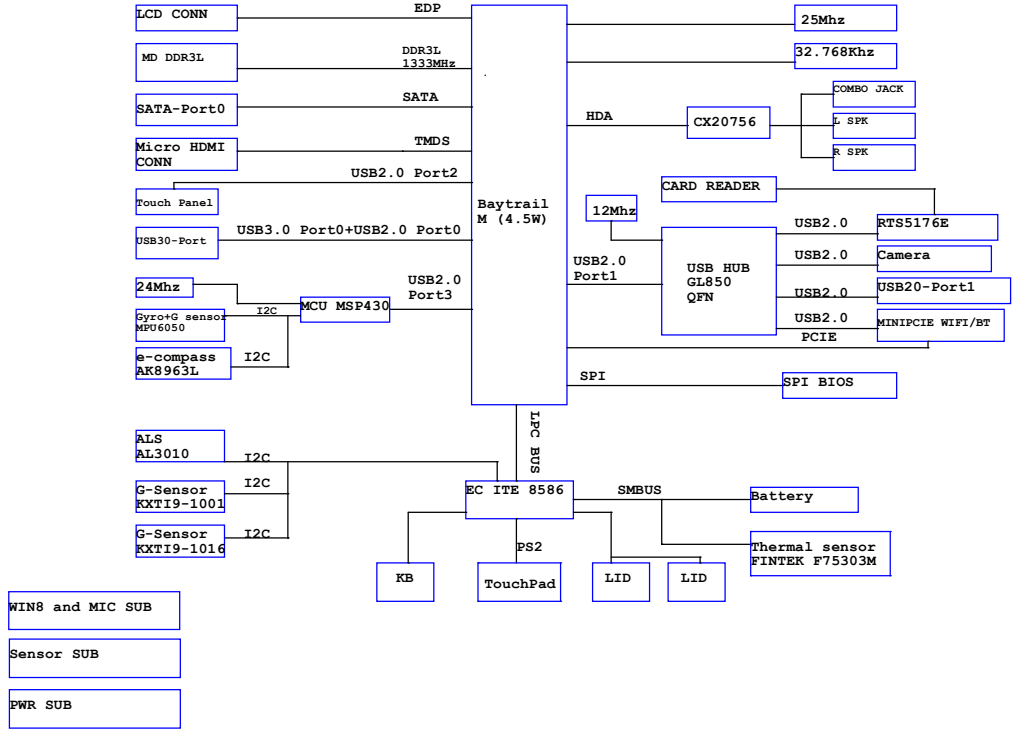
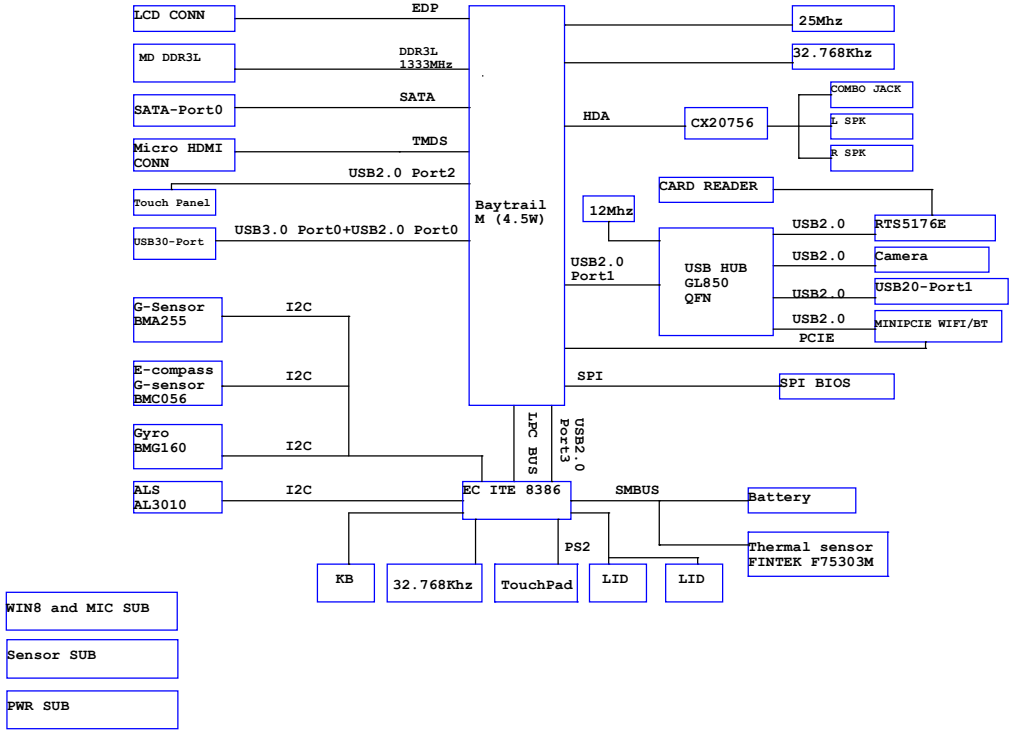
VIENNA M Block diagram
EC 8586



VIENNA M Block diagram
EC 8386



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Voltage Rails (O --> Means ON , X --> Means OFF)

State \ Power Plane	B+ +3VL	+3VALW +5VALW	+3VALW_SOC +1.0VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

SMBUS Control Table

	SOURCE	ALS	BATT	Thermal Sensor	G-sensor	G-sensor1	G-sensor2	E-compass	GYRO	TP Module
EC_SMB_CLK1 EC_SMB_DAT1	IT8586 +3VALW_EC	V +3VS	V +3VLP	X	V +3VS	X	X	X	X	X
EC_SMB_CLK2 EC_SMB_DAT2	IT8586 +3VS	X	X	V +3VS	X	X	X	X	X	X
EC_SMB_CLK3 EC_SMB_DAT3	IT8386 +3VS	X	X	X	X	V +3VS	V +3VS	V +3VS	V +3VS	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	X	X	X	V +3VS

SM Bus address

	Device	address
EC1	Battery	0001 011X b
	Charger	
	ALS	
	G-sensor	
EC2	Thermal Sensor	1001_101xb
EC3	G-sensor1	
	G-sensor2	
	E-compass	
	GYRO	
SOC	TP	

Red Block For 8386

PCIE PORT LIST

Port	Device
0	WLAN
1	X
2	X
3	X

USB Port Table

		USB20		USB30
EXPRESS CARD USB	0	Left USB	1	Left USB
	1	USB HUB		
	2	TOUCH PANEL		
	3	MCU		
USB HUB	1	Right USB		
	2	CAMERA		
	3	CARD READER		
	4	WLAN		

BOM Structure Table

BOM Structure	DA8@	HDMI@	USB30@	RF@	EMC@	45@				
BOM Structure										

Board ID Table

Board ID	Description	PCB Revision

BOM Configuration Table

SKU	Description	BOM Config	
SKU1	Intel I3-4010Y 1.3G ULX 6W 2+2 QS	45:HDMI@	
		43:DA8@,4100@,RF@	
SKU2	Intel I5-4200Y 1.4G ULX 6W 2+2 QS	45:HDMI@	
		43:DA8@,4200@,RF@	

X76&VGA Configuration Table

SKU	Description	BOM Config	

Vinafix

PCB And LOGO Config

	CPU	PCB	LOGO
NPI DA8xxxxx	ZZZ5 N2910@ ZZZ4 N3510@ ZZZ6 N2810@ S IC FH8065301546401 QF9D B1 1.6GS 1170FH8065301546300 QF9E B1 2G BGA FH8065301564500 QF9F B1 2G BGA 1170 PCB 0T5 NM-A201 REV0 M/B	ZZZ DA8@	
MP DAZxxxxx			

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Title: Notes List

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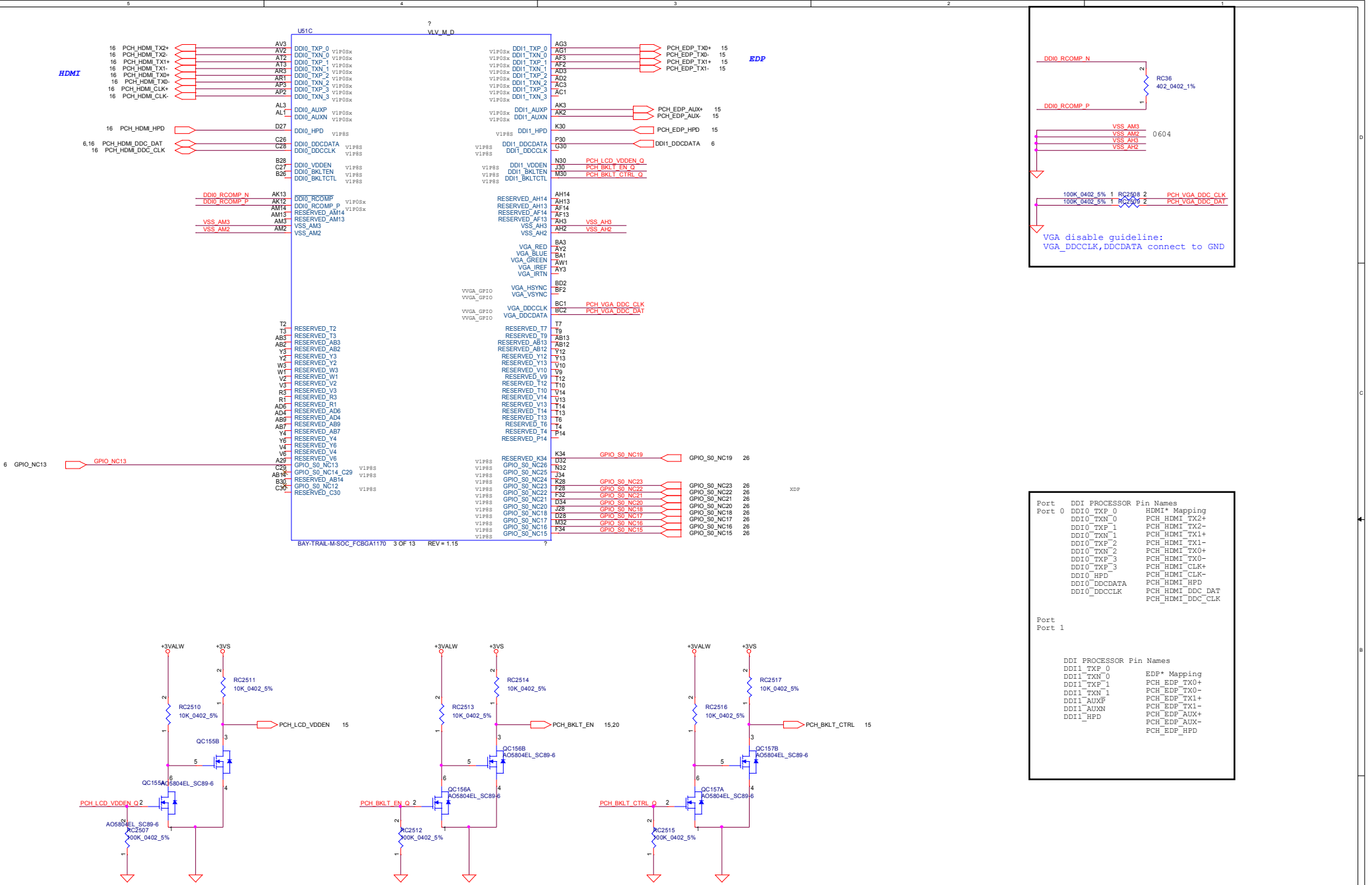

Port DDI PROCESSOR Pin Names

Port		
Port 0	DDI0_TXP_0	HDMI* Mapping
	DDI0_TXN_0	PCH_HDMI_TX2+
	DDI0_TXP_1	PCH_HDMI_TX2-
	DDI0_TXN_1	PCH_HDMI_TX1+
	DDI0_TXP_2	PCH_HDMI_TX1-
	DDI0_TXN_2	PCH_HDMI_TX0+
	DDI0_TXP_3	PCH_HDMI_TX0-
	DDI0_TXP_3	PCH_HDMI_CLK+
	DDI0_HPD	PCH_HDMI_CLK-
	DDI0_DDCDATA	PCH_HDMI_HPD
	DDI0_DDCCLK	PCH_HDMI_DDC_DAT
		PCH_HDMI_DDC_CLK
Port		
Port 1		

DDI PROCESSOR Pin Names

DDI1_TXP_0	
DDI1_TXN_0	EDP* Mapping
DDI1_TXP_1	PCH_EDP_TX0+
DDI1_TXN_1	PCH_EDP_TX0-
DDI1_AUXP	PCH_EDP_TX1+
DDI1_AUXN	PCH_EDP_TX1-
DDI1_HPD	PCH_EDP_AUX+
	PCH_EDP_AUX-
	PCH_EDP_HPD

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DDRA_DQ[63:0] 12
DDRA_MA[15:0] 12
DDRA_DQS[7:0] 12
DDRA_DQS#[7:0] 12
DDRA_DM[7:0] 12

DDRB_DQ[63:0] 13
DDRB_MA[15:0] 13
DDRB_DQS[7:0] 13
DDRB_DQS#[7:0] 13
DDRB_DM[7:0] 13

U51A — VLV_M_D — 1 OF 13 — BAY-TRAIL-M-SOC_FCBGA1170 REV = 1.15

U51B — VLV_M_D — 2 OF 13 — BAY-TRAIL-M-SOC_FCBGA1170 REV = 1.15

Del CS_2(chip select: 1 per Rank)
Del CKE_2(chip select: 1 per Rank)

For dual rank

100K_0402_1% RC212 ICLK_DRAM_TERMN_0
100K_0402_1% RC224 ICLK_DRAM_TERMN_1

DDR_PWROK
DDR_CORE_PWROK

SM_RCOMP_0
SM_RCOMP_1
SM_RCOMP_2

DRAM_VREF

+1.35V
RC886 4.7K_0402_1%
RC138 0_0402_5%
RC887 4.7K_0402_1%
CC217 .1U_0402_10V6-K

SM_RCOMP_2
SM_RCOMP_1
SM_RCOMP_0
RC34 23.2_0402_1%
RC33 29.4_0402_1%
RC35 162_0402_1%

DDR3 Compensation Signal
WIDTH:20MIL
SPACING: 25MIL
Length: 500Mil

+3VALW
+1.35V
RC257 10K_0402_5%
RC254 10K_0402_5%
RC139 0_0402_5%
DDR_PWROK
QC193B 2N7002KDWH_SOT363-6
CC219 .1U_0402_10V6-K
20,32 VR_VDDQ_PWRGD
QC193A 2N7002KDWH_SOT363-6
CC218 .1U_0402_10V6-K

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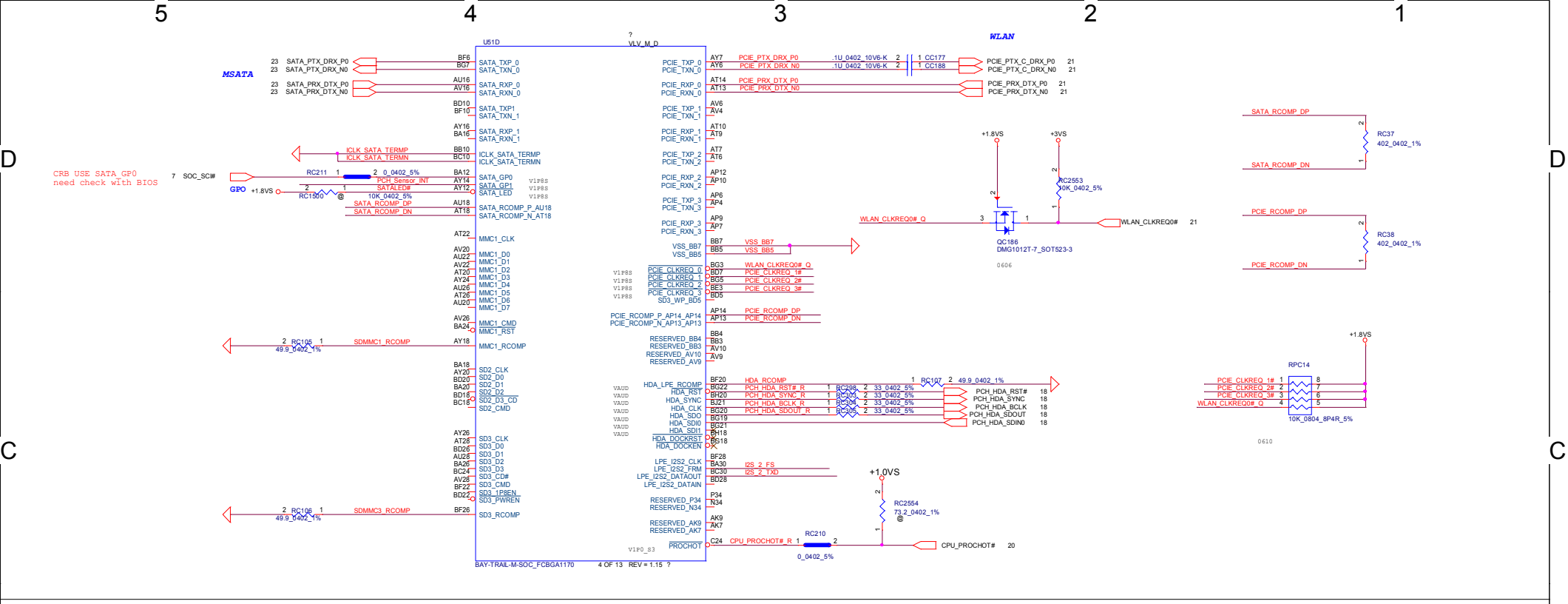

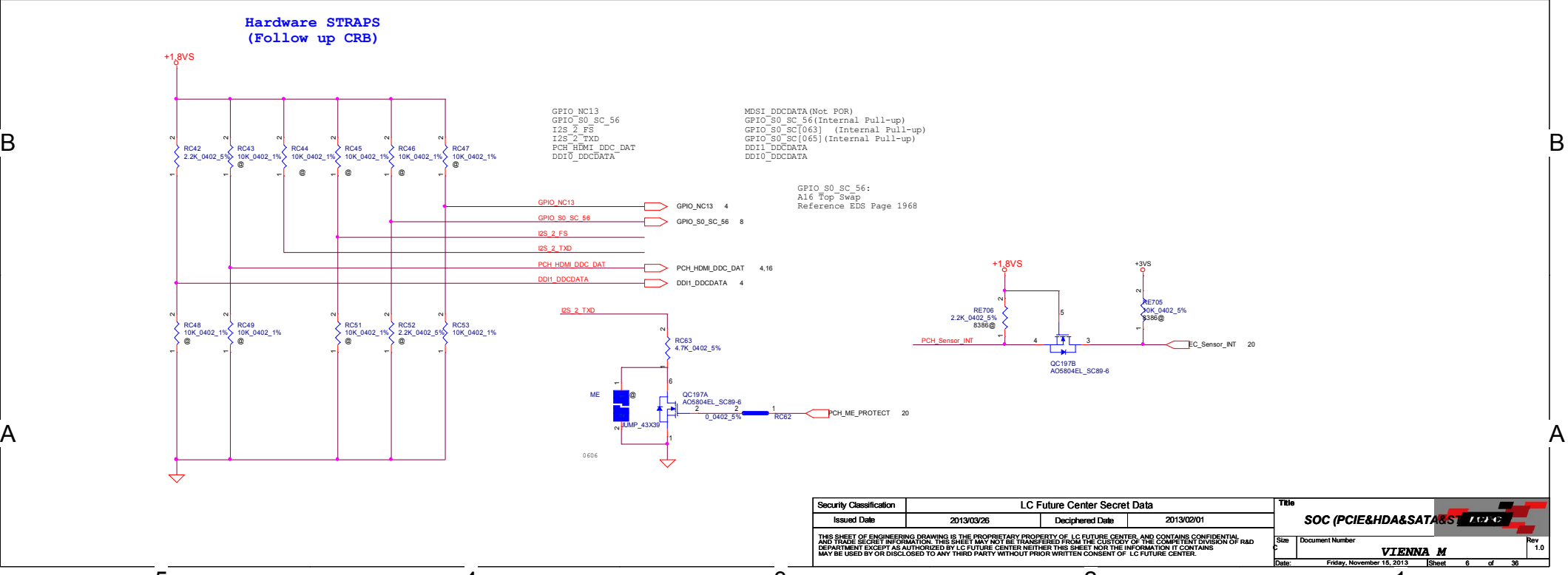

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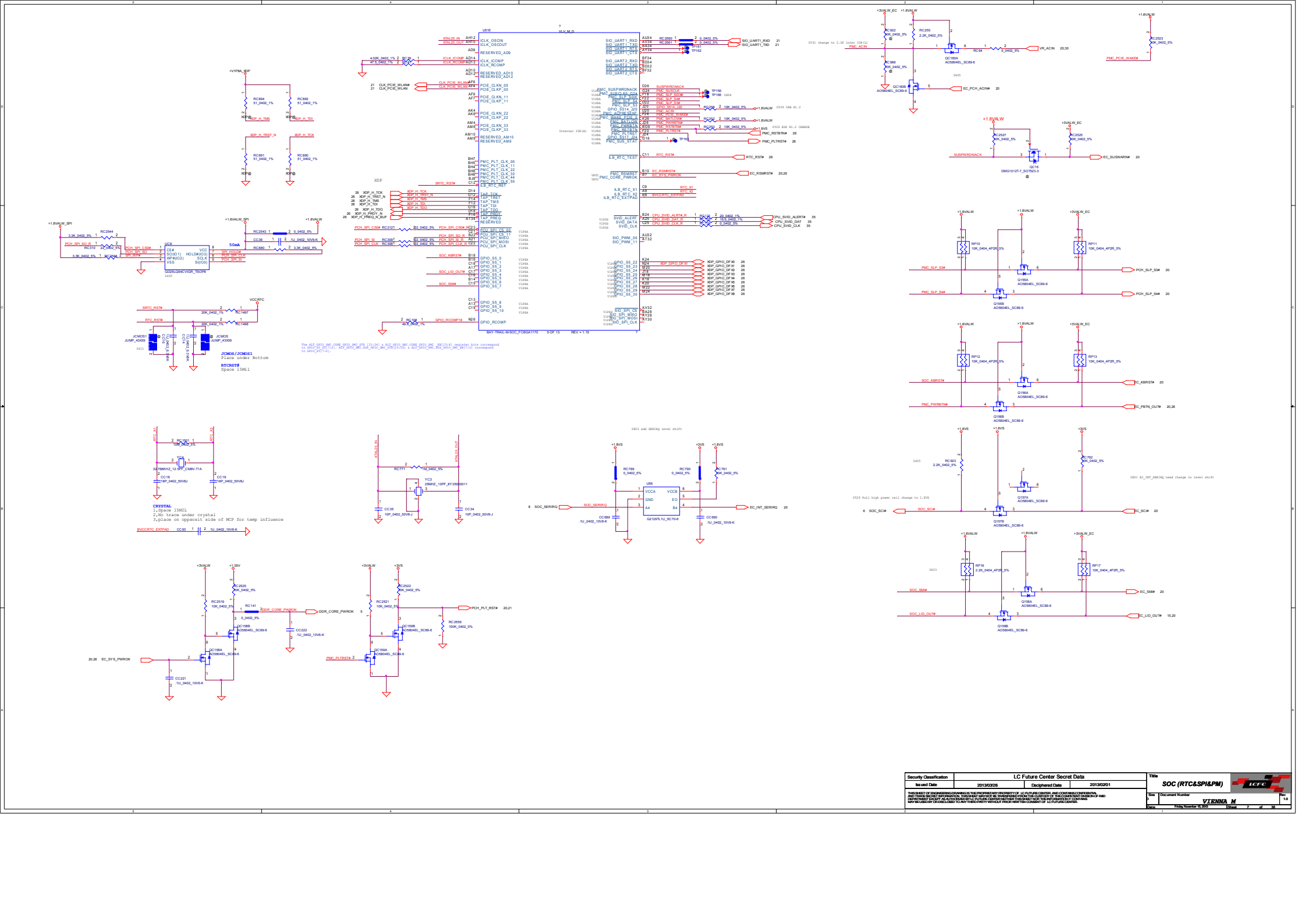
U51E
BAY-TRAIL-M-SOC_FCBGA1170
5 OF 13
REV = 1.15
JCMOS0/JCMOS1
Place under Bottom
RTCRST#
Space 15Mil
CRYSTAL
1.Space 15MIL
2.No trace under crystal
3.place on opposit side of MCP for temp influence
32.768KHZ_12.5PF_CMBV-T1A
BAT54C_SOT23
50mA
LD05LG54CVGR_TSOP6
QC16
DMG1012T-7_SOT523-3
QC160A
AO5804EL_SC89-6
QC160B
AO5804EL_SC89-6
QC155A
AO5804EL_SC89-6
QC155B
AO5804EL_SC89-6
QC156A
AO5804EL_SC89-6
QC156B
AO5804EL_SC89-6
QC157A
AO5804EL_SC89-6
QC157B
AO5804EL_SC89-6
QC158A
AO5804EL_SC89-6
QC158B
AO5804EL_SC89-6
QC159A
AO5804EL_SC89-6
QC159B
AO5804EL_SC89-6
U56
G2129TL1U_SC70-6
XDP
0531 change to 2.2K inter 20K(L)
0529 Pull high power rail change to 1.8V3
0803 add SERIRQ level shift
0803 EC_INT_SERIRQ need change to level shift
The ALT_GPIO_SMI_CORE_GPIO_SMI_STS [31:24] & ALT_GPIO_SMI_CORE_GPIO_SMI_EN[31:24] & ALT_GPIO_SMI_MUX_GPIO_SMI_SEL[31:0] correspond to GPIO[95:64].
Internal 20K(H)
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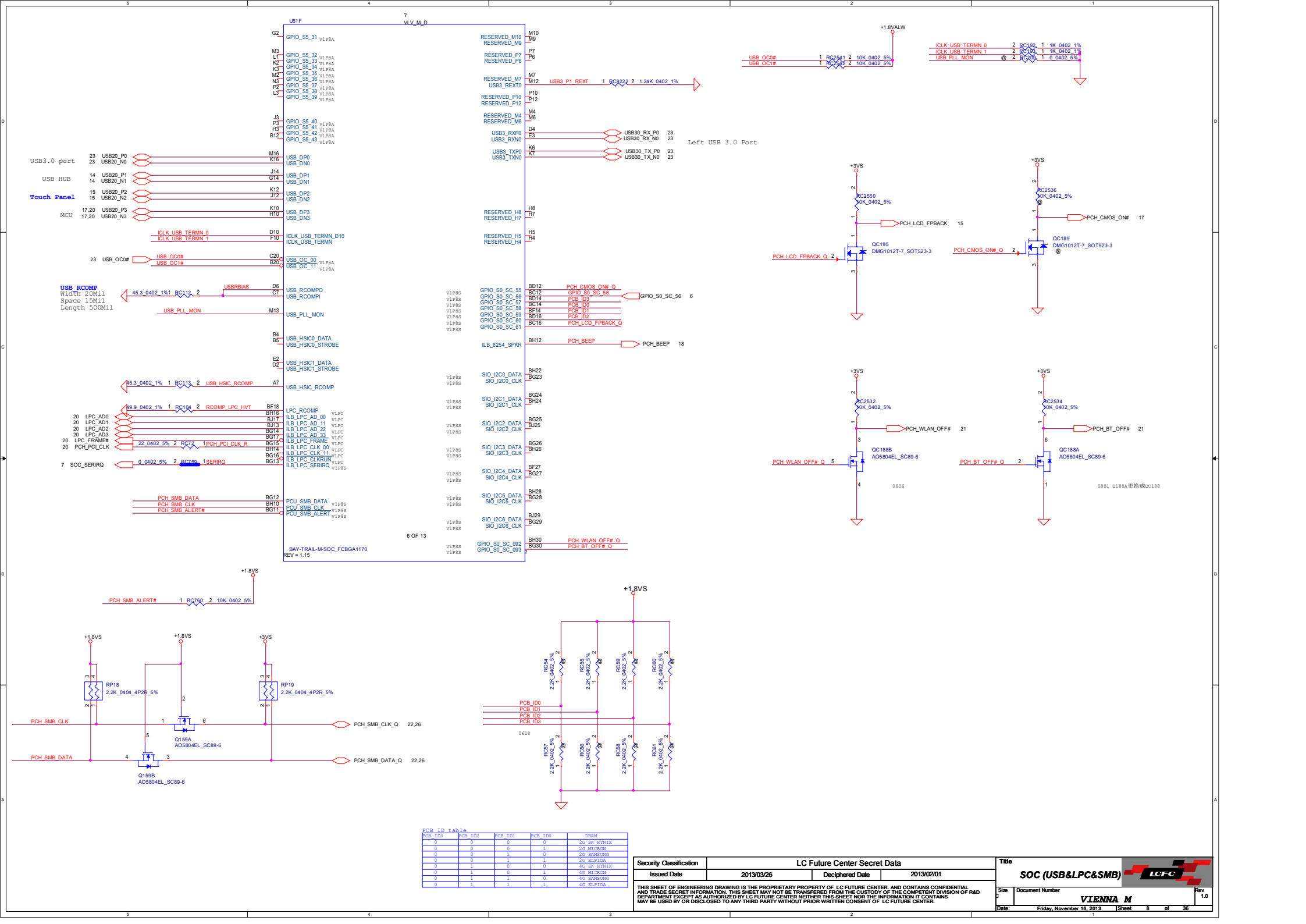

PCB_ID table

PCB_ID3	PCB_ID2	PCB_ID1	PCB_ID0	DRAM
0	0	0	0	2G_SK HYNIX
0	0	0	1	2G_MICRON
0	0	1	0	2G_SAMSUNG
0	0	1	1	2G_ELPIDA
0	1	0	0	4G_SK HYNIX
0	1	0	1	4G_MICRON
0	1	1	0	4G_SAMSUNG
0	1	1	1	4G_ELPIDA

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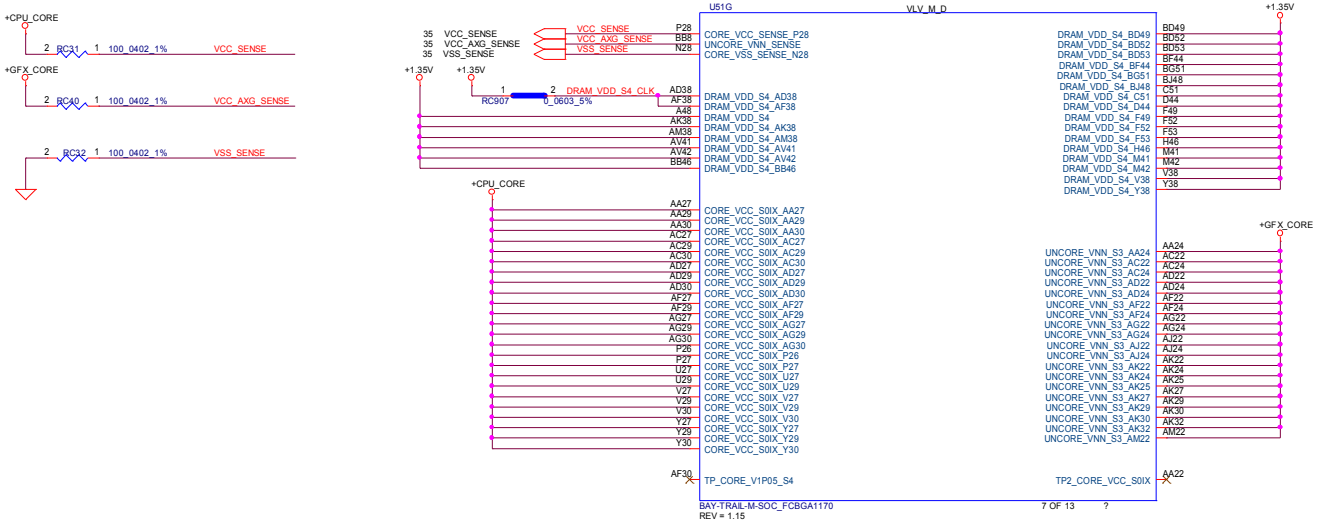

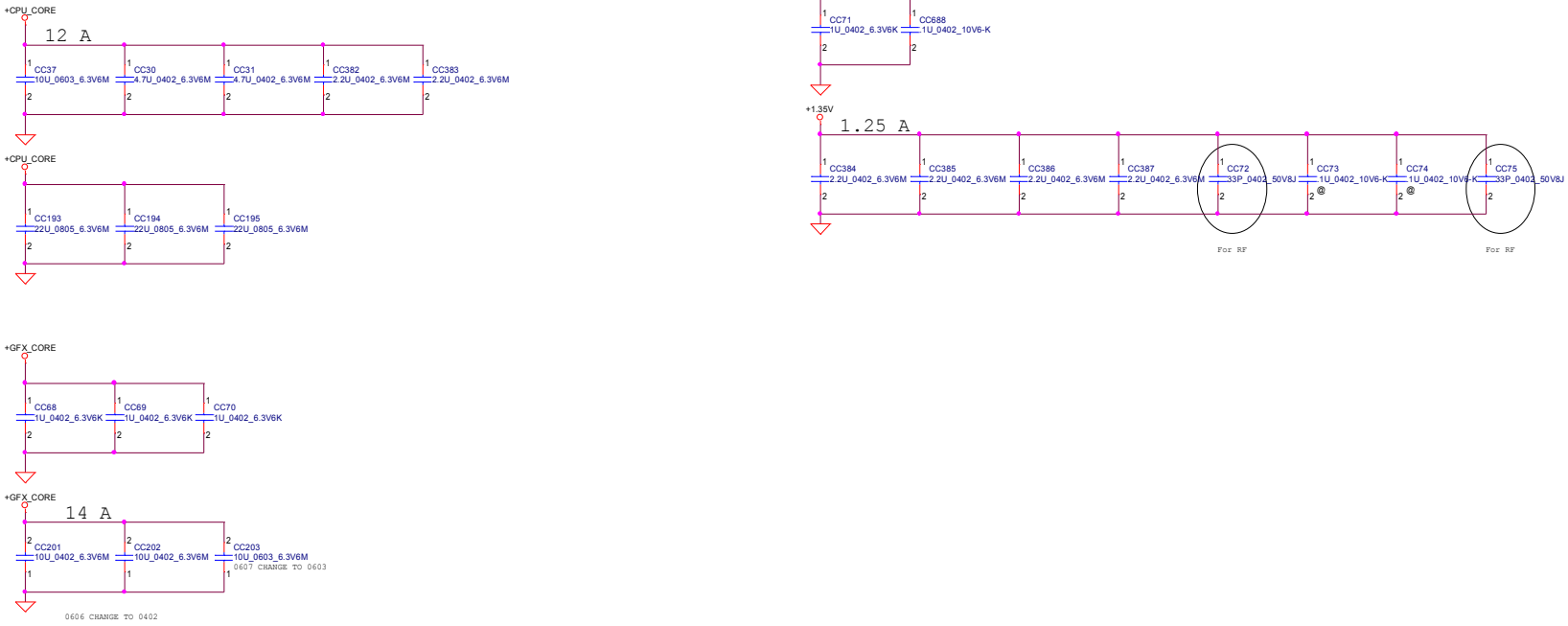

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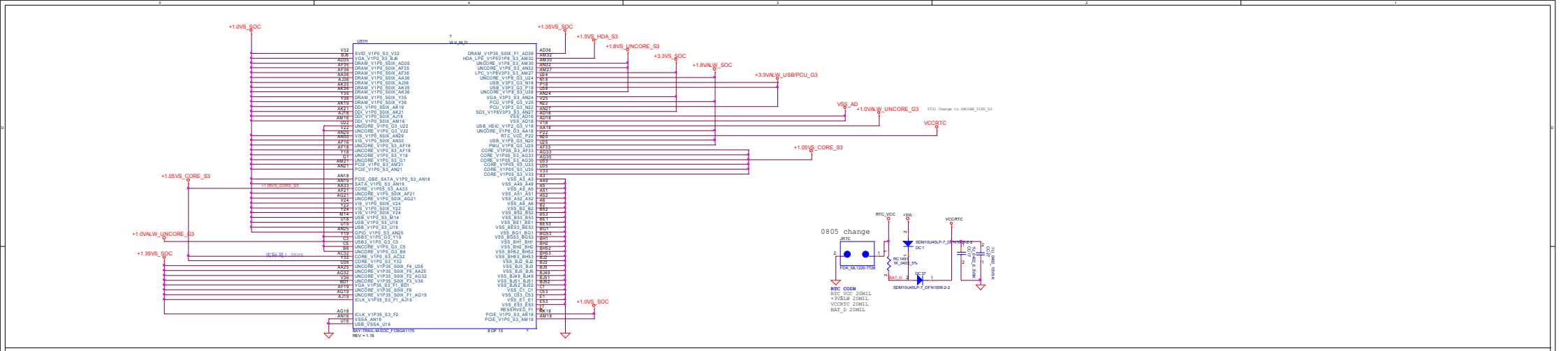

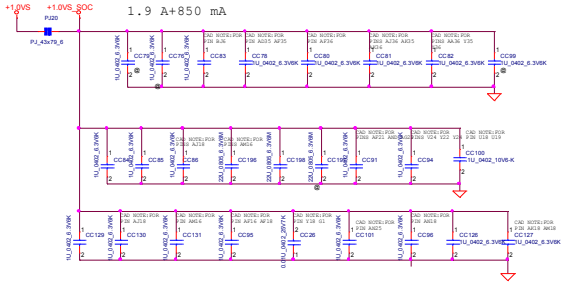

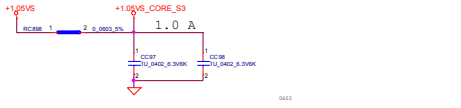

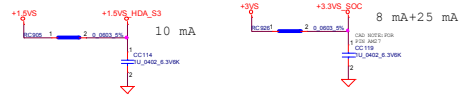

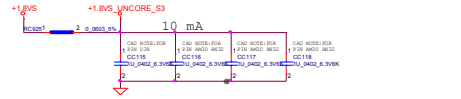

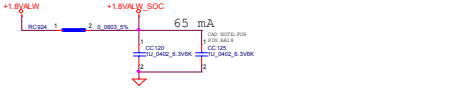

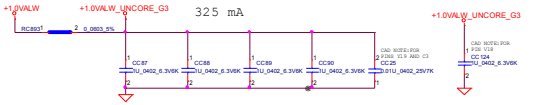

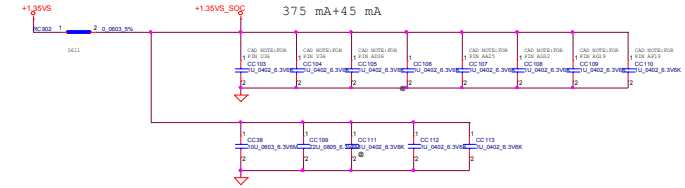

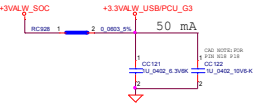

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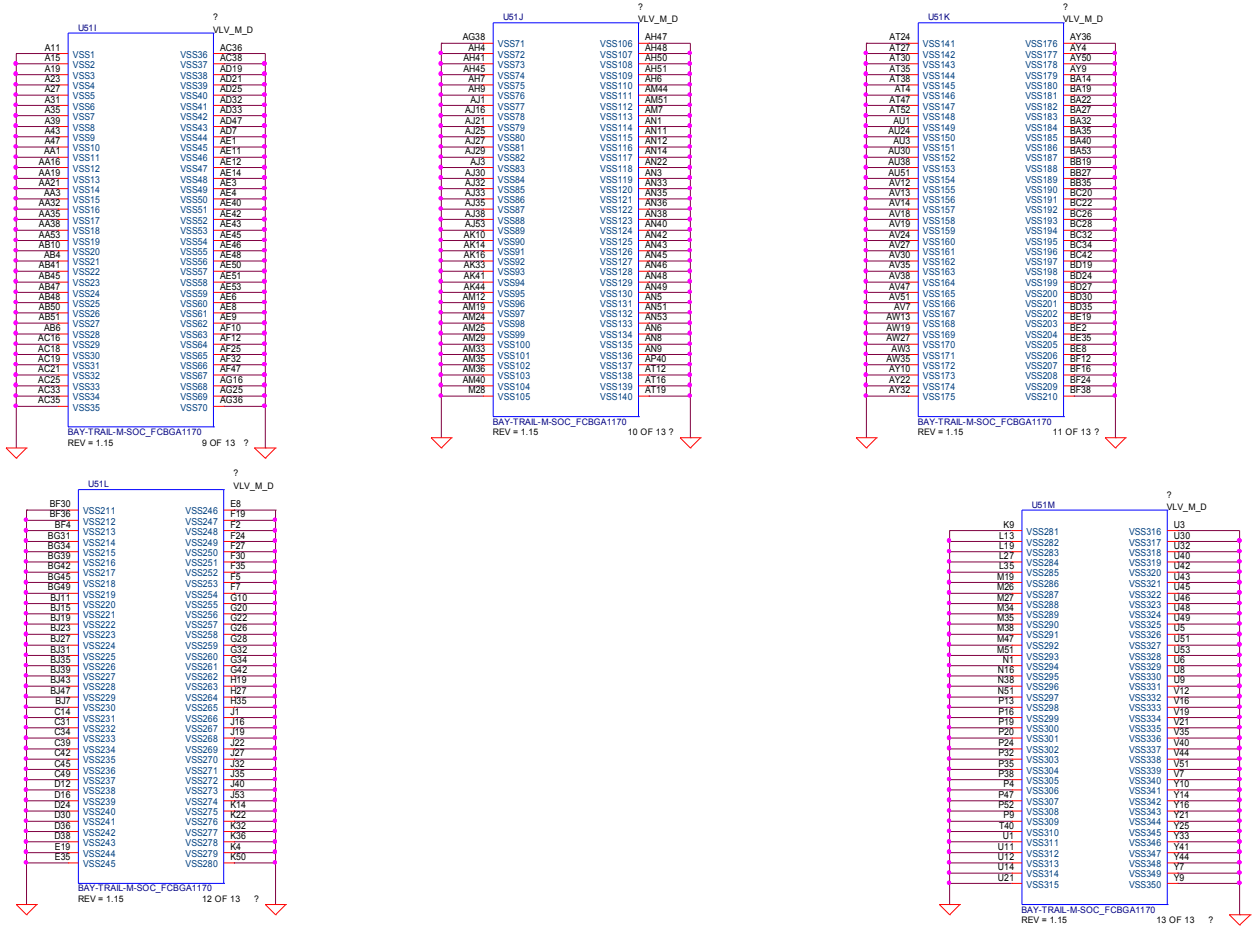

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Signal voltage level = 0.675 V
PLACE TWO 4.7K RESISTORS CLOSE TO
DIMMS ON DIMM_VREF_CA / DIMM_VREF_DQ
Decoupling caps are needed; one 0.1 µF placed close to VREF pins

Trace width:20 mils
Space:20mils

Need change to 36ohm 5%

Need change to 36ohm 5%

Need change to 39ohm 5%

change 0.2pf

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Issued Date	2012/12/14	Deciphered Date	2012/12/21

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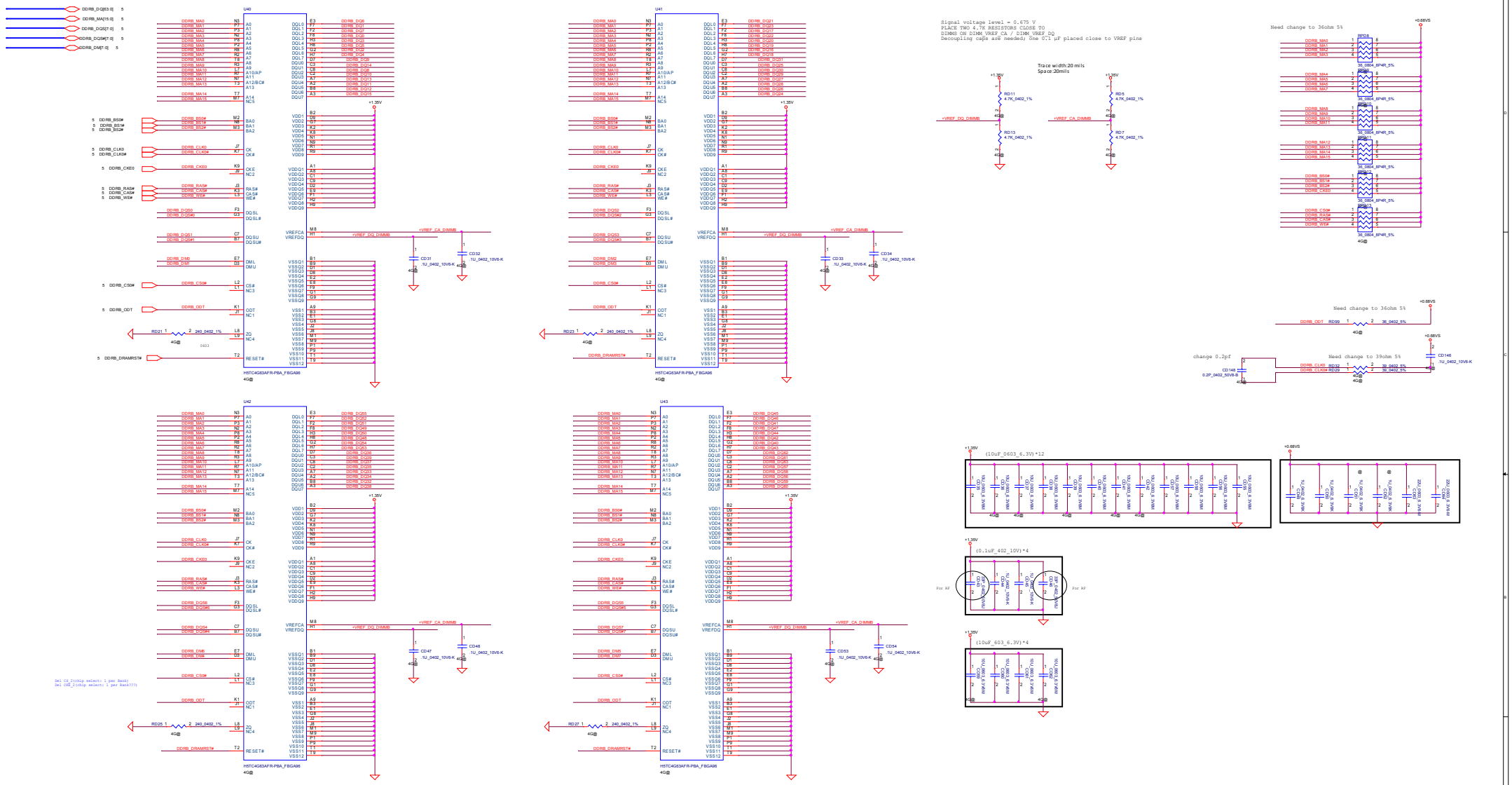
Title: DDR3L

Size: D | Document Number: VIENNA M | Rev: 1.0

Date: Friday, November 16, 2012 | Sheet 12 of 36



Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2013/02/01

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Title: DDR3L

Size: D | Document Number: VIENNA M | Rev: 1.0

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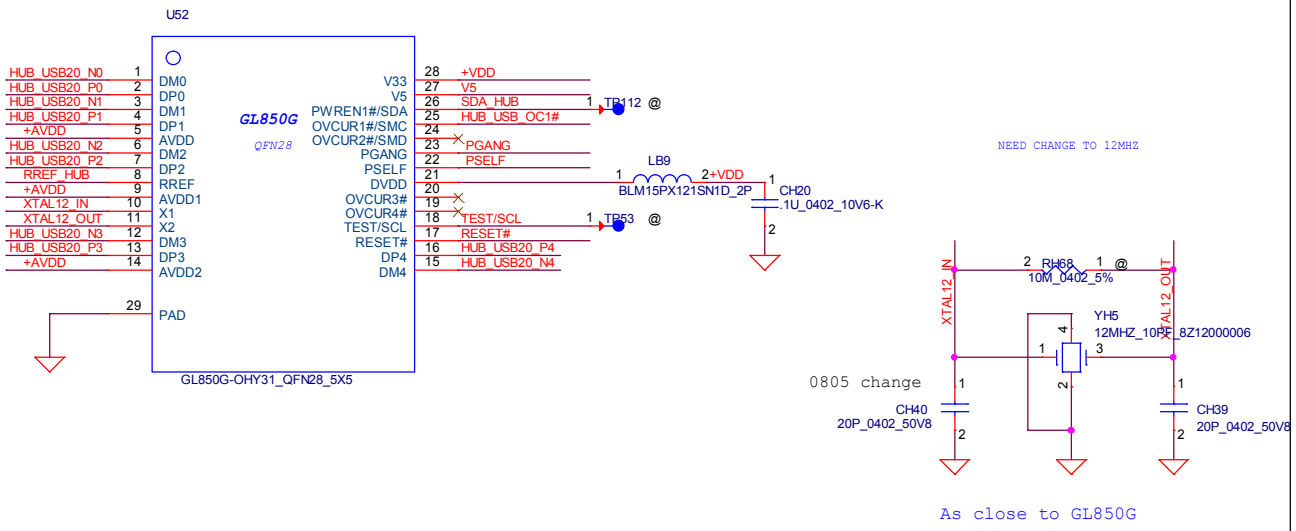

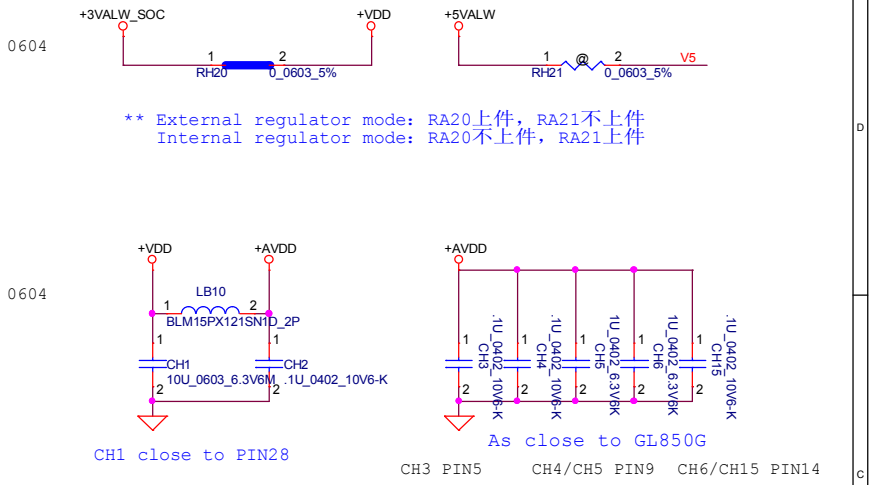

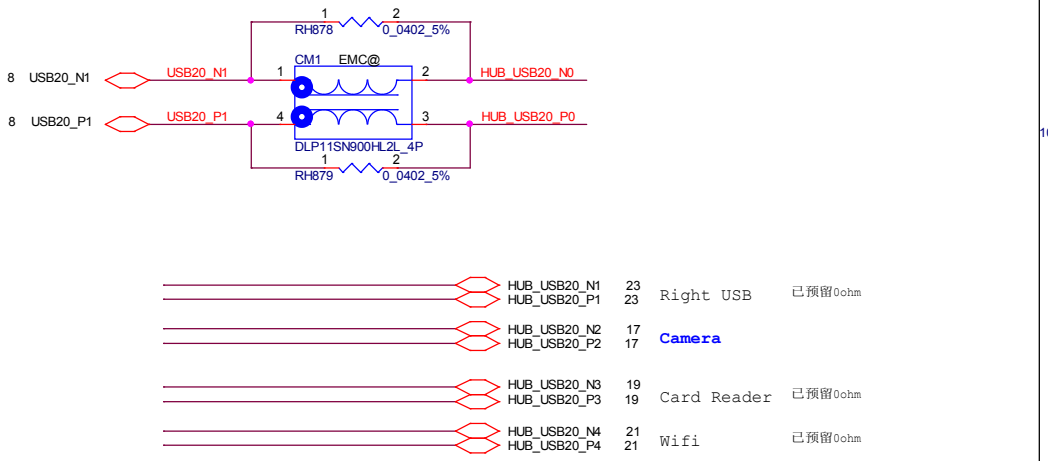

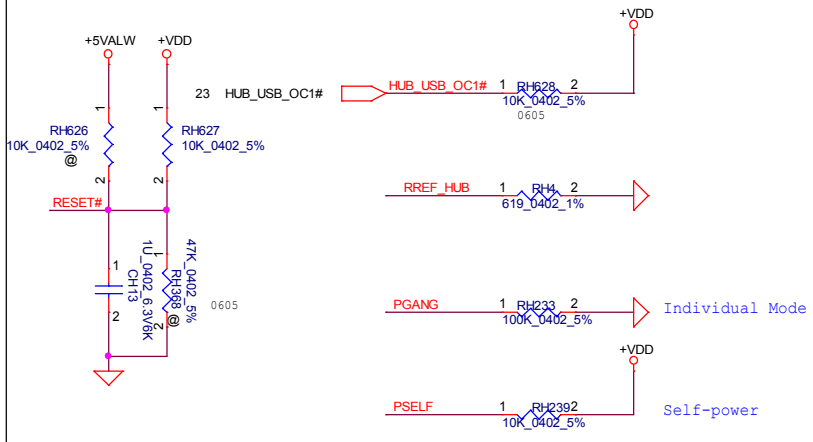

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Title: USB Hub GL850G-OHY31

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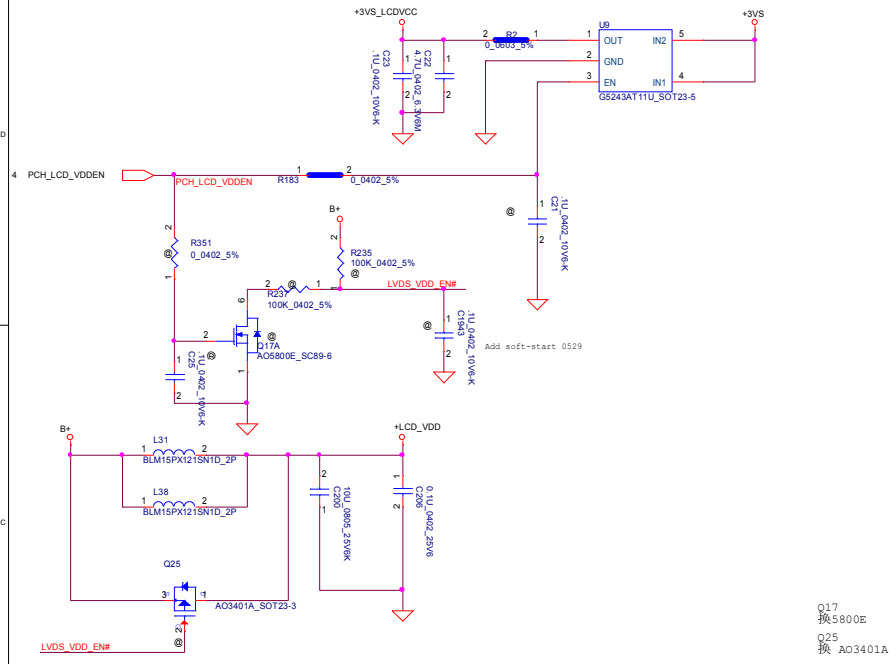
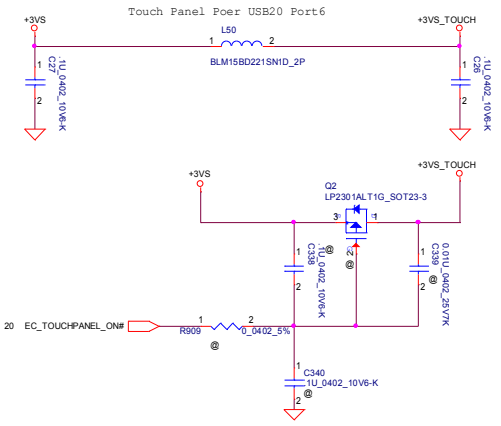
LCD PWR

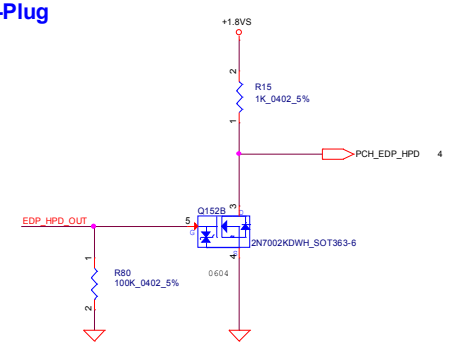


Q17
AO5800E
Q25
AO3401A

TOUCH PANEL



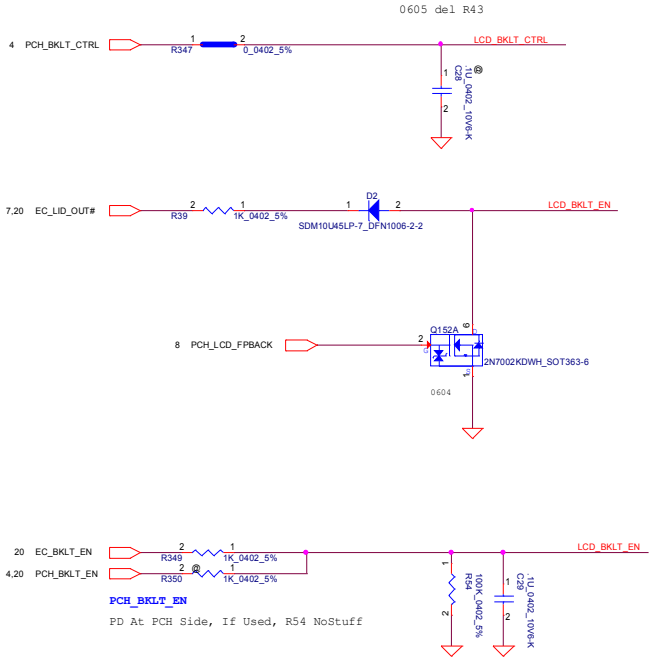
Hot-Plug



EDP_HPD

*EDP EN,EDP-HPD EN
EDP EN, EDP-HPD Disabled, 10K PU Via VCCIO
EDP Disabled, NC

BKLT CNTL



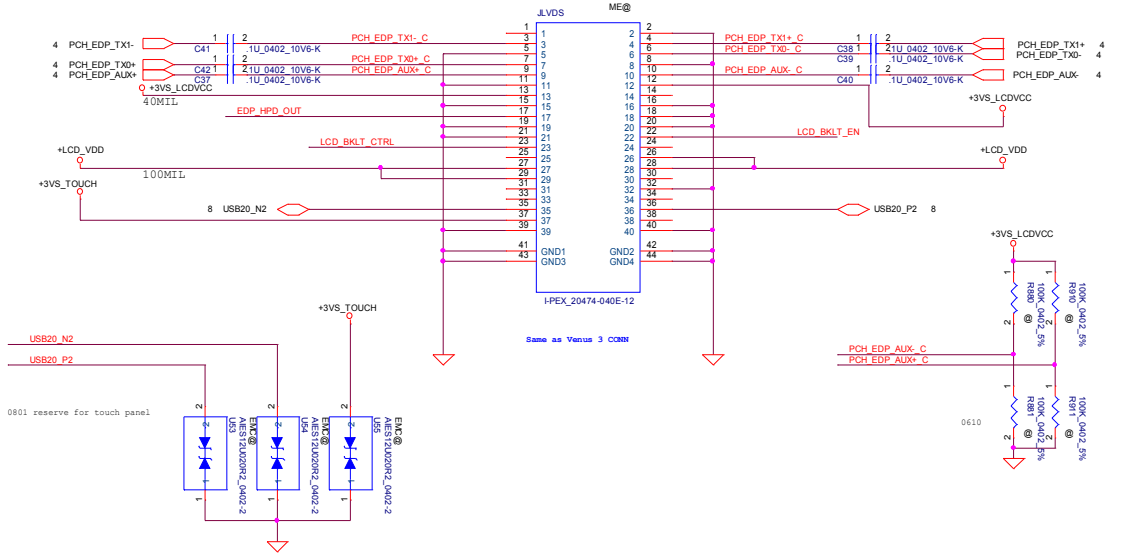
PCH_BKLT_EN

PD At PCH Side, If Used, R54 NoStuff

CONN

LCDVCC
Width 40Mil

LCDVDD
Width 100Mil



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Title			
LCD			
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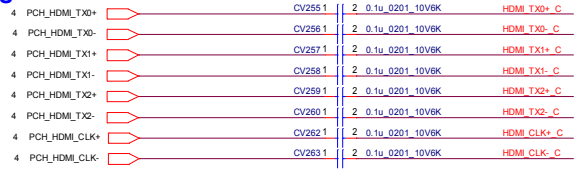
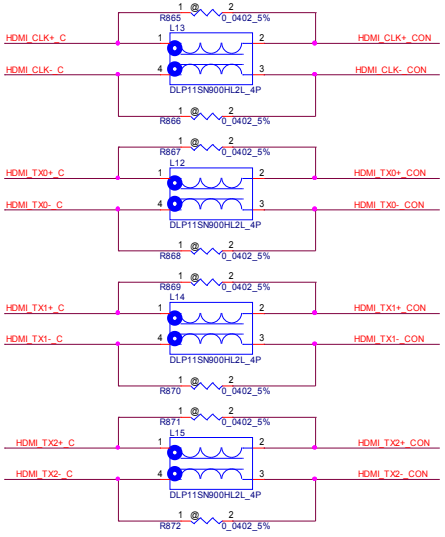
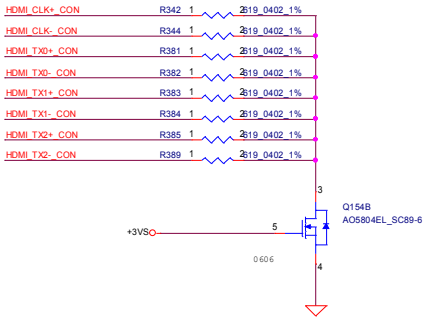
TMDS







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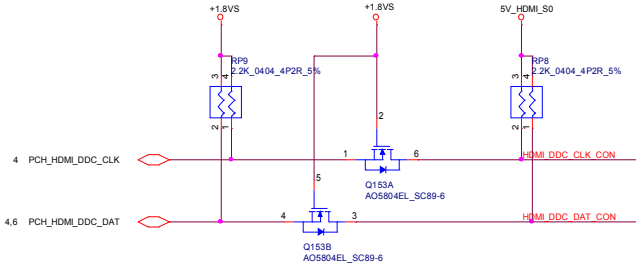
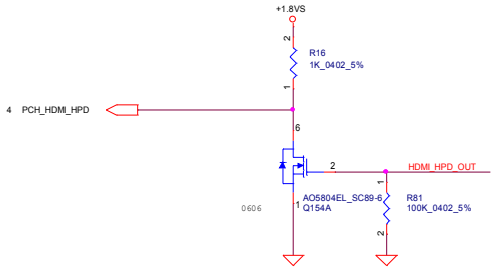
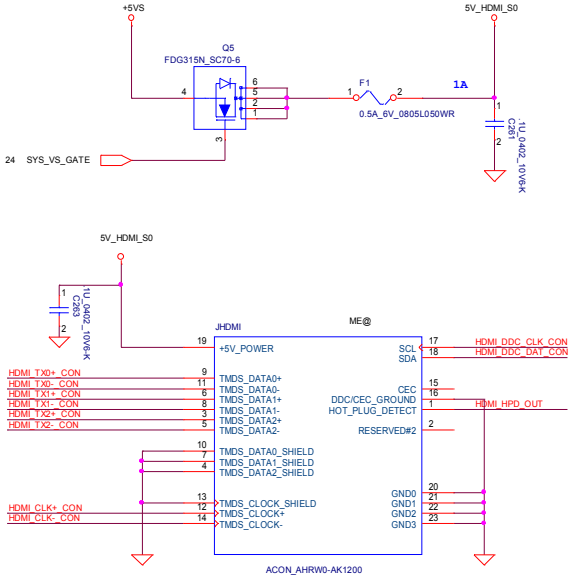


H-PLUG

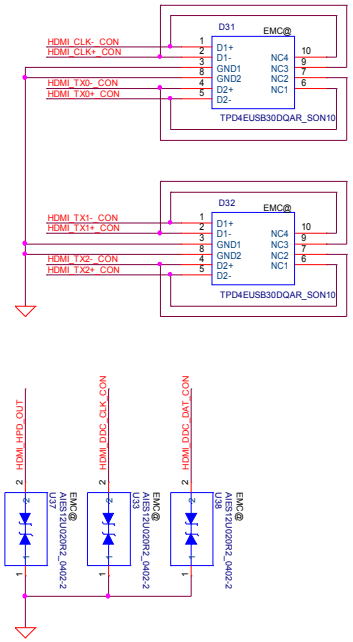


CONN



New Symbol

ESD



Note

1. Mount0ohm resistor,Reserve choke

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Title	HDMI		
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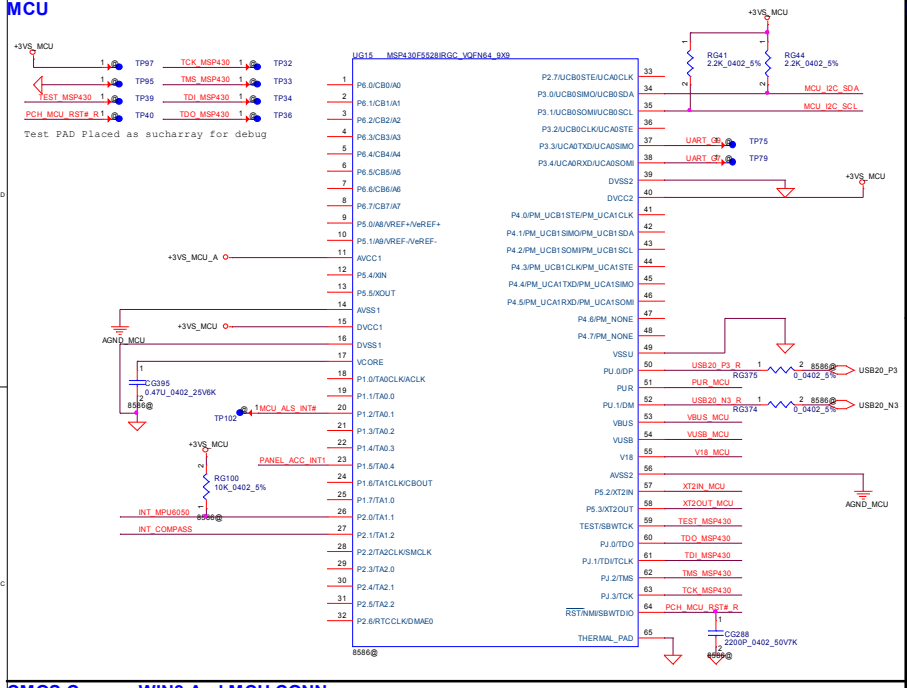
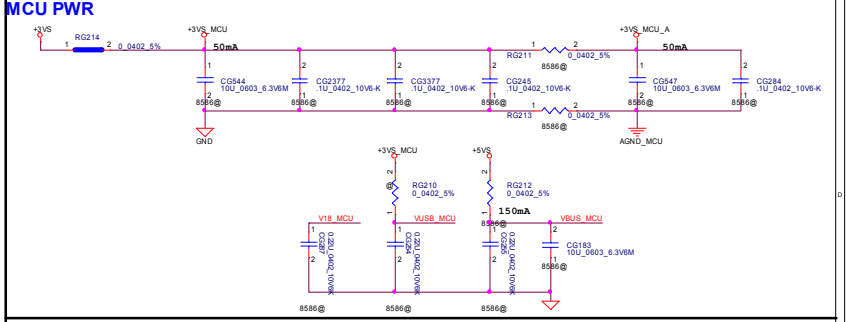
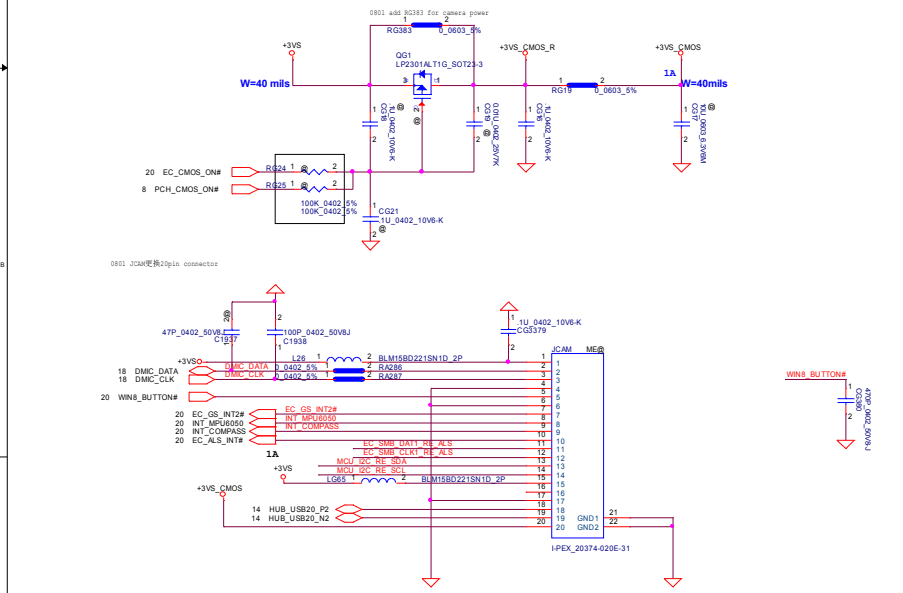
MCU



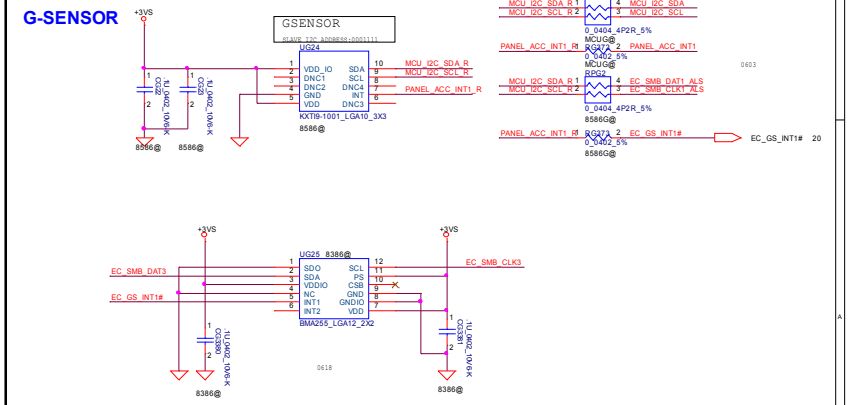
MCU PWR



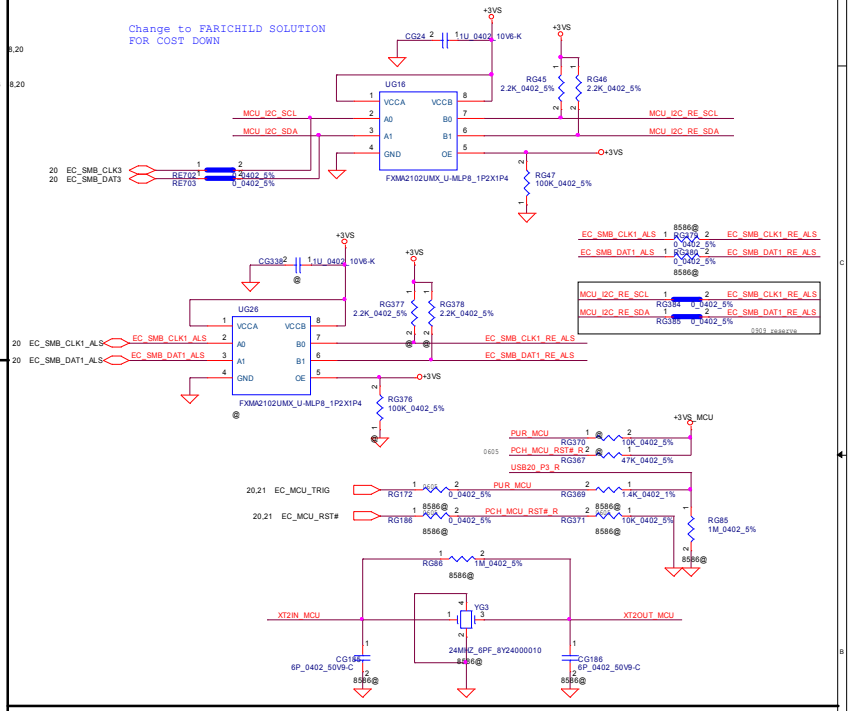
CMOS Camera WIN8 And MCU CONN



G-SENSOR



Change to FARICHILD SOLUTION FOR COST DOWN



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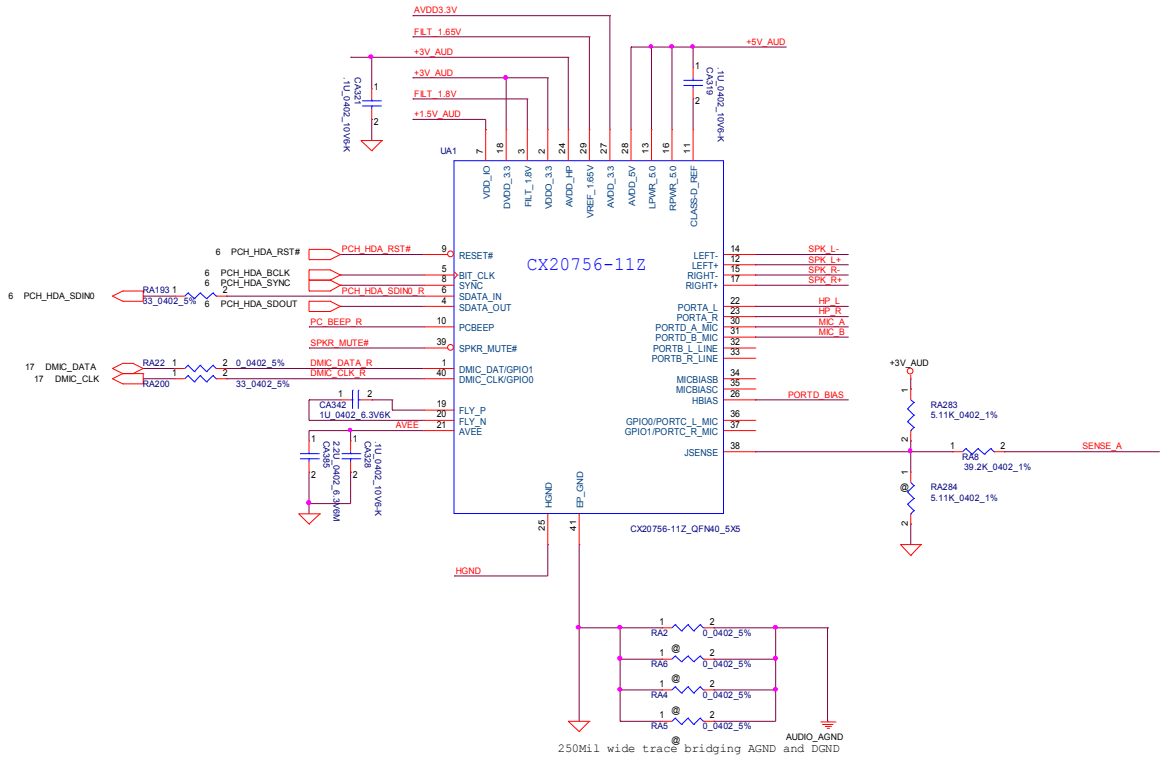
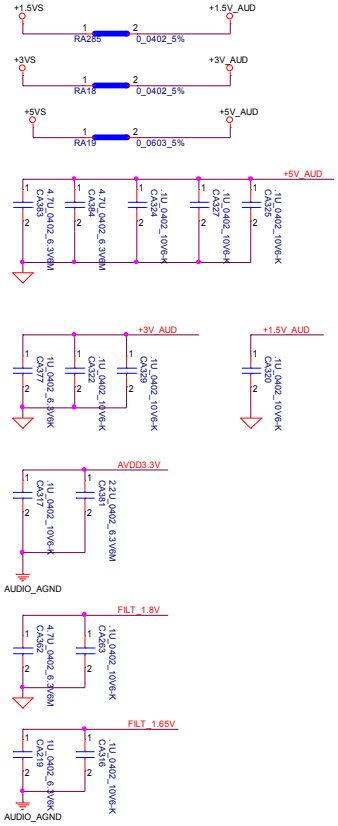
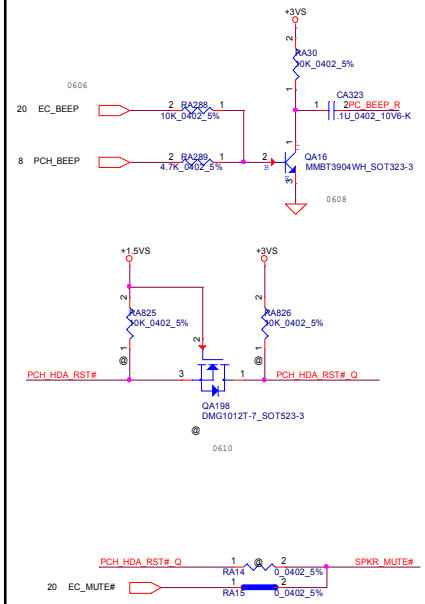
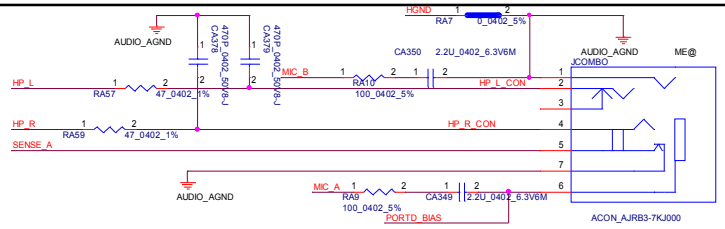
CODEC



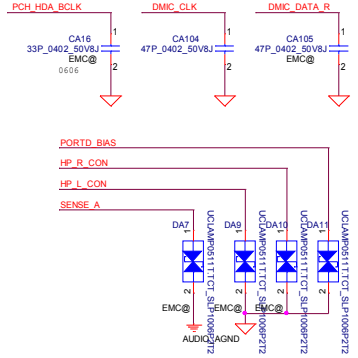




COMBO Jack

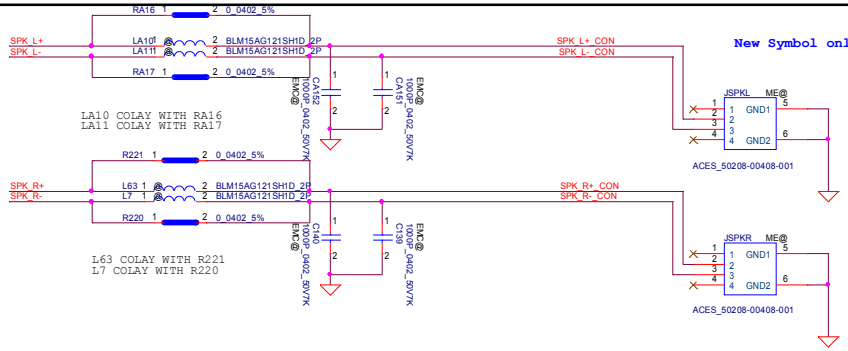


New Symbol

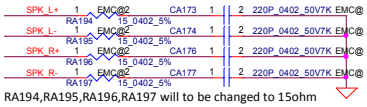


Left

Right



New Symbol only use 2pin



RA194,RA195,RA196,RA197 will to be changed to 15ohm

Place Close To Codec

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Title	AUDIO		
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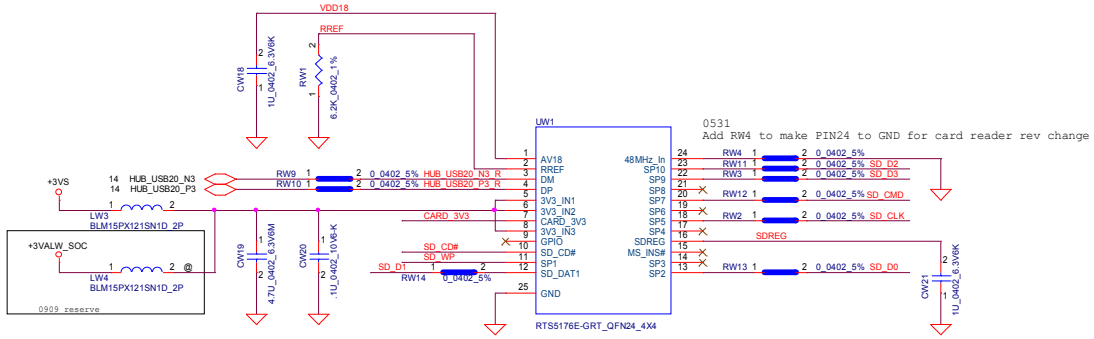
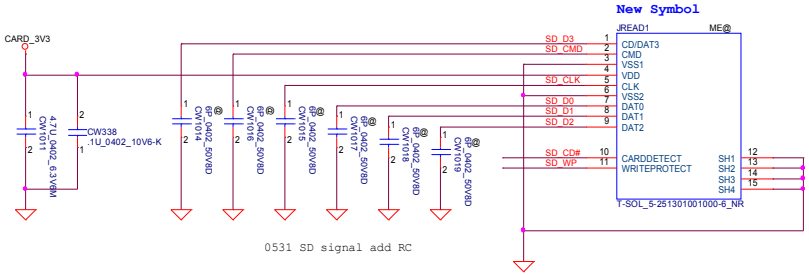
CARD READER





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Title	Cardreader		
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C	VIENNA M		1.0
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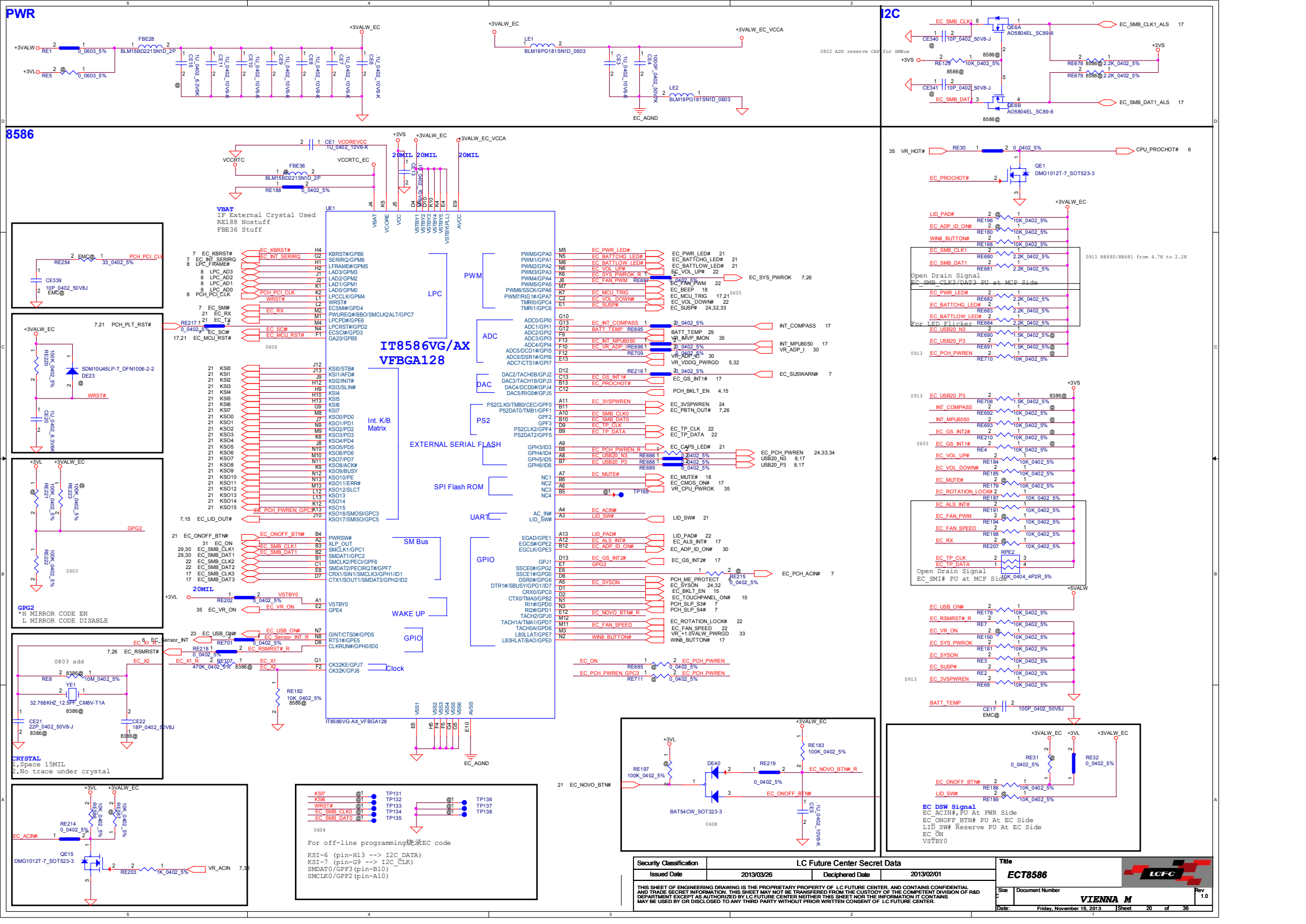
PWR
I2C
8586
IT8586VG/AX
VFBGA128
LPC
PWM
ADC
DAC
PS2
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
GPIO
SM Bus
WAKE UP
Int. K/B Matrix
Clock
VBAT
IF External Crystal Used
RE188 Nostuff
FBE36 Stuff
EC_SYS_PWROK
INT_COMPASS
INT_MPU6050
EC_SUSWARN#
EC_PCH_PWREN
EC_PCH_ACIN#
EC_NOVO_BTN#
CPU_PROCHOT#
EC_SMB_CLK1_ALS
EC_SMB_DAT1_ALS
Open Drain Signal
EC_SMB_CLK3/DAT3 PU at MCP Side
For LED Flicker
Open Drain Signal
EC_SMI# PU at MCP Side
EC DSW Signal
EC_ACIN#,PU At PWR Side
EC_ONOFF_BTN# PU At EC Side
LID_SW# Reserve PU At EC Side
EC_ON
VSTBY0
GPG2
*H MIRROR CODE EN
L MIRROR CODE DISABLE
CRYSTAL
1,Space 15MIL
2,No trace under crystal
For off-line programming MCU EC code
KSI-6 (pin-H13 --> I2C_DATA)
KSI-7 (pin-G9 --> I2C_CLK)
SMDAT0/GPF3(pin-B10)
SMCLK0/GPF2(pin-A10)
0802 ADD reserve CAP for SMBus
0911 RE680/RE681 from 4.7K to 2.2K
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LC Future Center Secret Data
Issued Date
2013/03/26
Deciphered Date
2013/02/01
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ECT8586
Size
C
Document Number
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Rev
1.0
Date:
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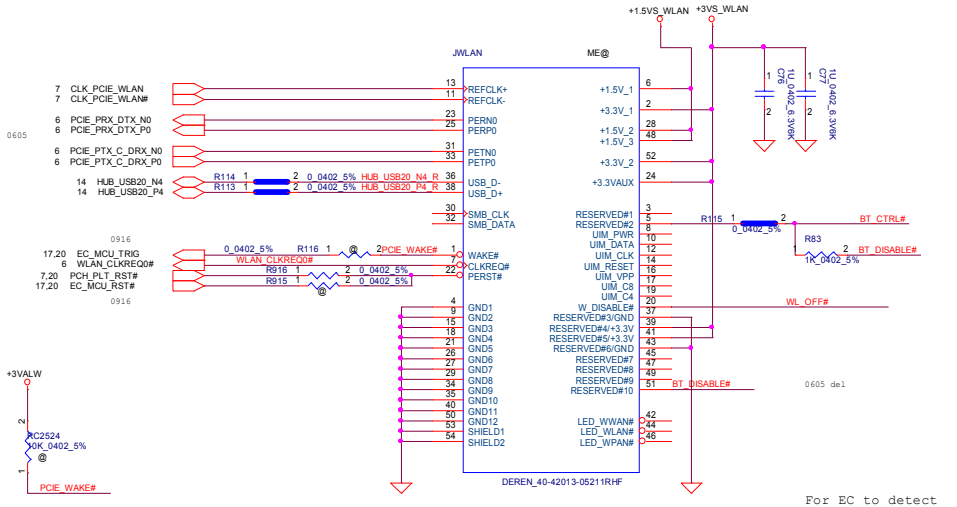
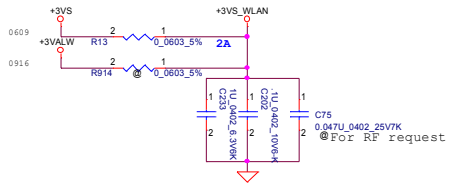
WIFI&BT Board Connector

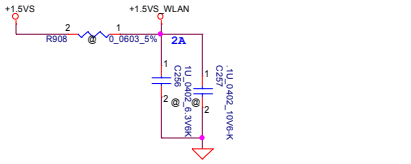
Mini Card(WLAN/WiMAX)

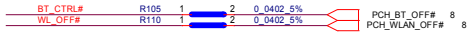


New Symbol

For EC to detect
debug card insert.







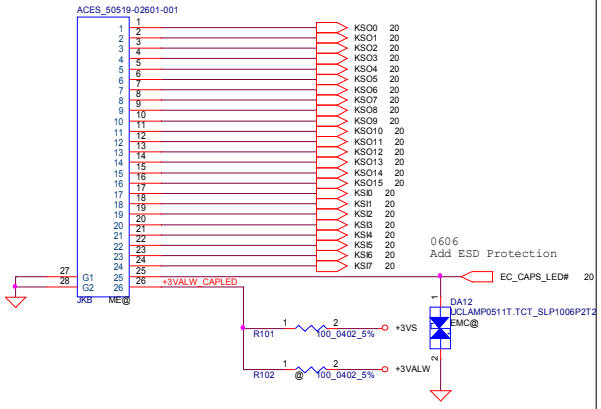
Mini Card
Connector Pin define确认
Current: Half Card???

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
* BT_CRTL (GPIO22)	H	L
PCH_BT_ON#	L	H

Keyboard Connector

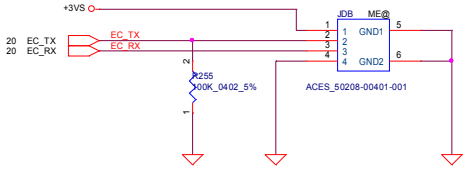
Inverter



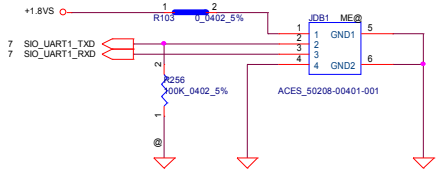
need add 4pin connector for 背光键盘

UART Debug Connector

For BIOS debug

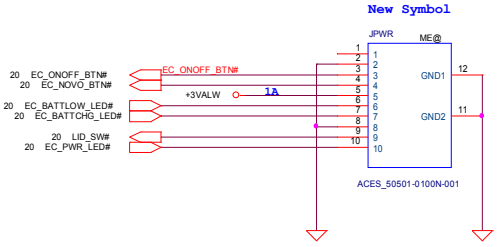


For Android OS debug



Power&Volume Board Connector

New Symbol



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Issued Date	2013/03/26	Deciphered Date	2013/02/01

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Title	CONN(WLAN&KB&PWRB&UA		
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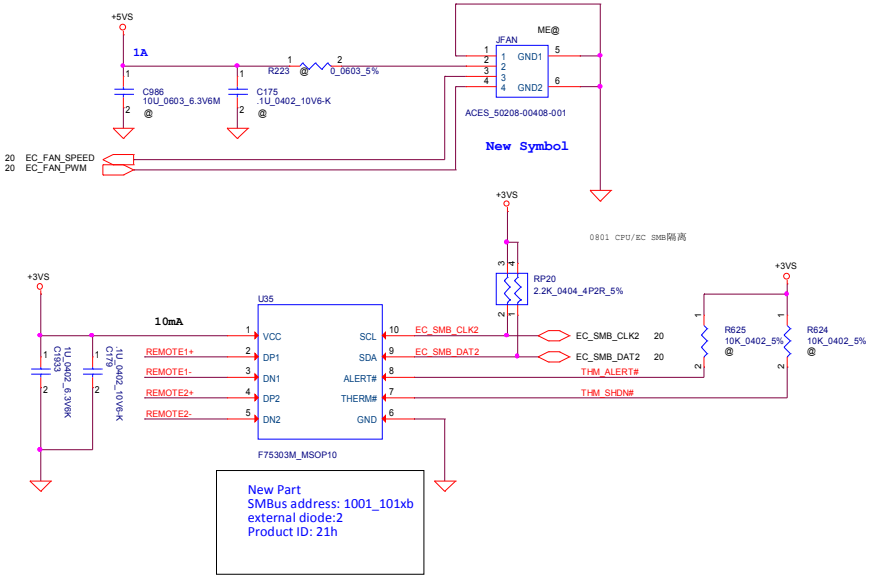

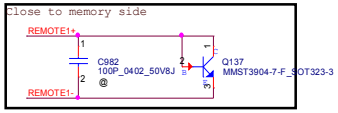

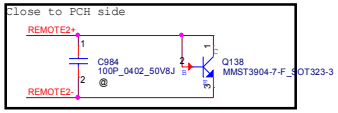

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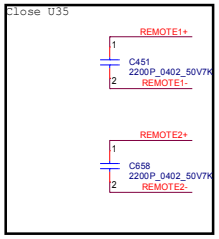
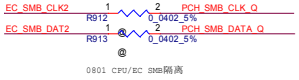
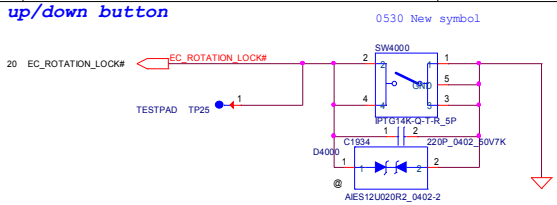
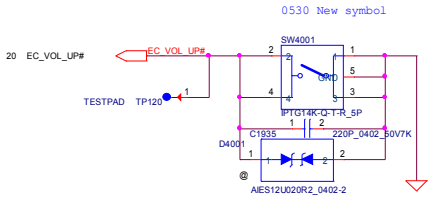
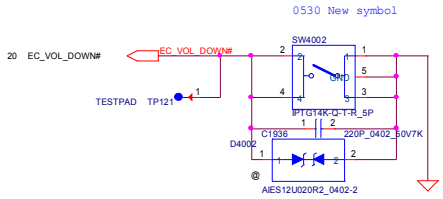




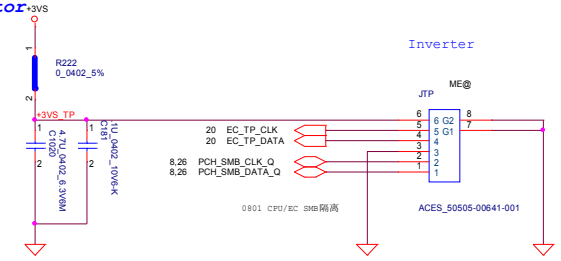
Rotation Vol up/down button







Touch Pad Connector



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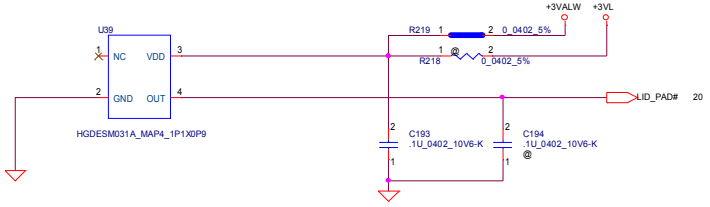

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Title: CONN(THM&FAN&RTN&SPKR)

Size	Document Number	Rev
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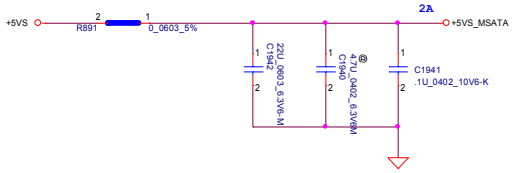
MSATA (Full Card)

0731 删除+3VS_MSATA线路



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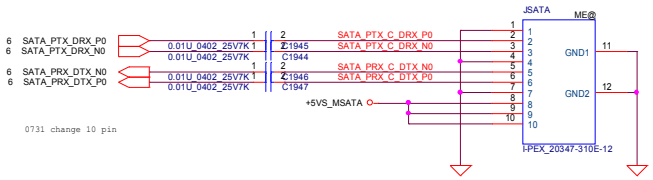
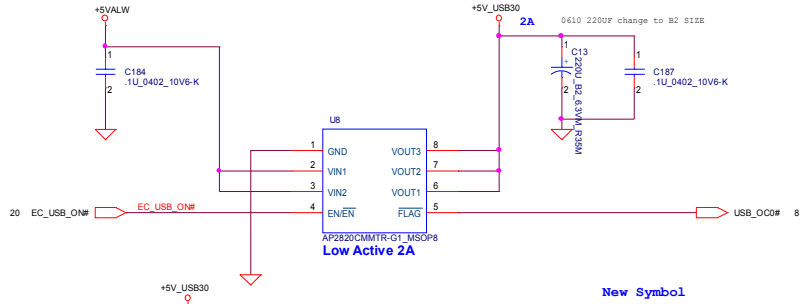


0731 change 10 pin

USB30



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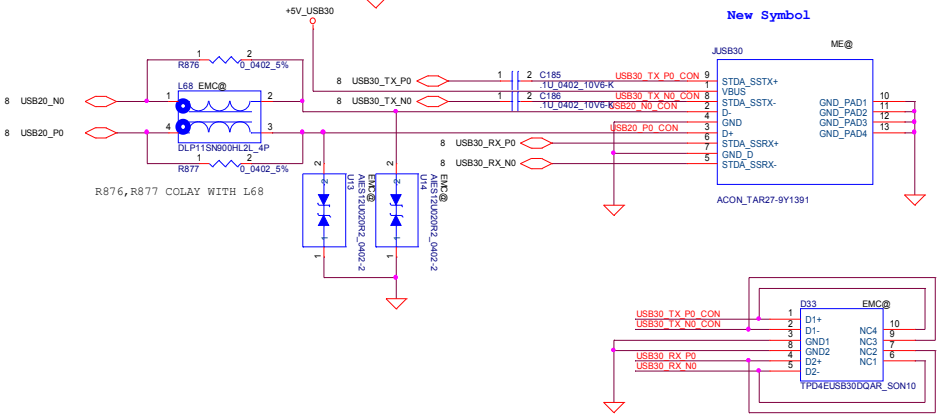
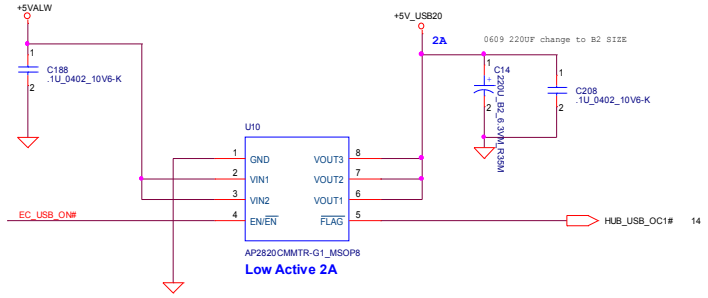
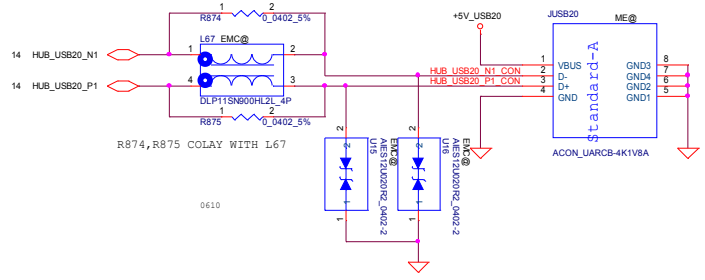


USB20





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Issued Date	2013/03/26	Deciphered Date	2013/02/01

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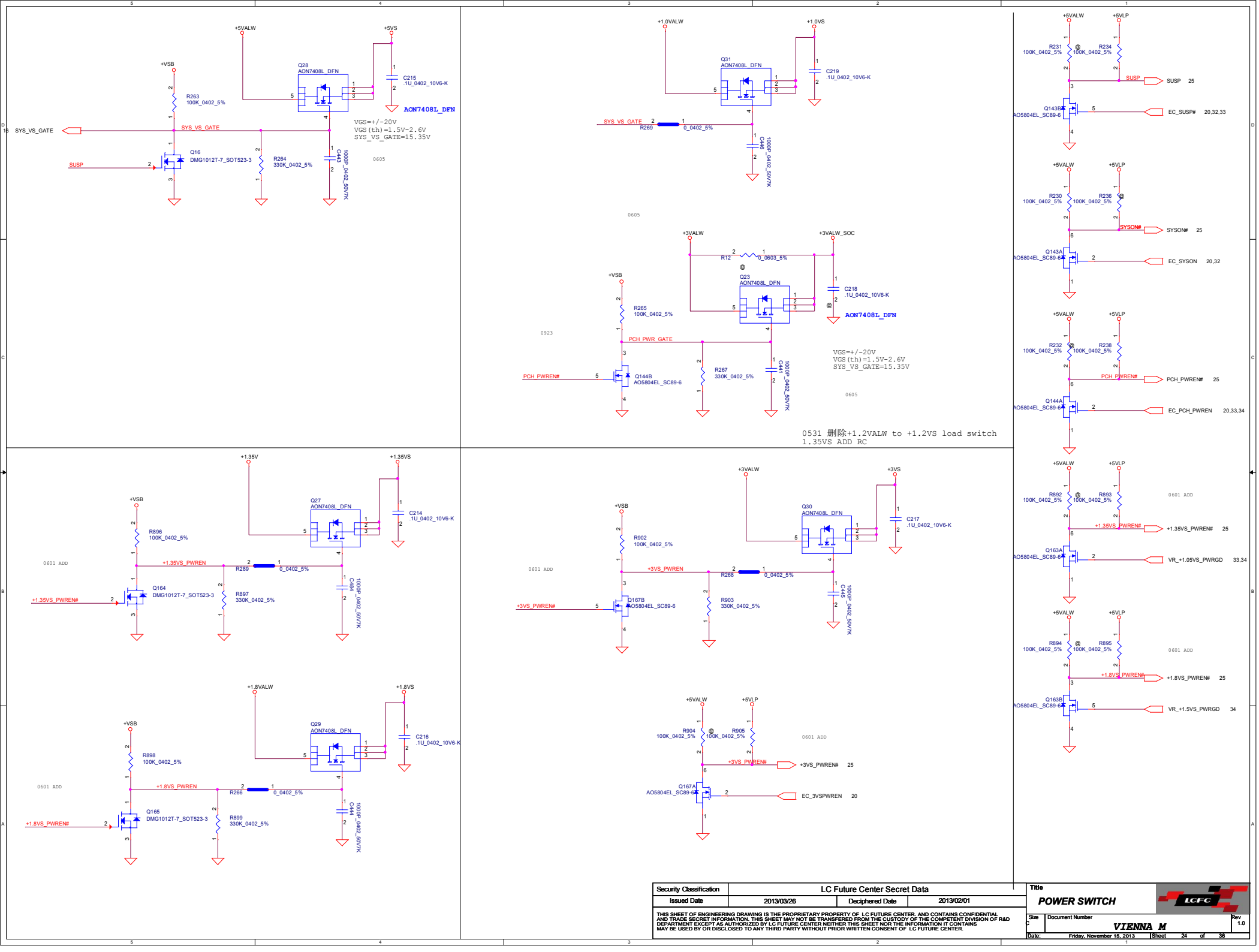
Size	Document Number		Rev
C	VIENNA M		1.0
Date:	Friday, November 15, 2013	Sheet	23 of 36



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Title: **POWER SWITCH**

Size	Document Number	Rev
C	VIENNA M	1.0
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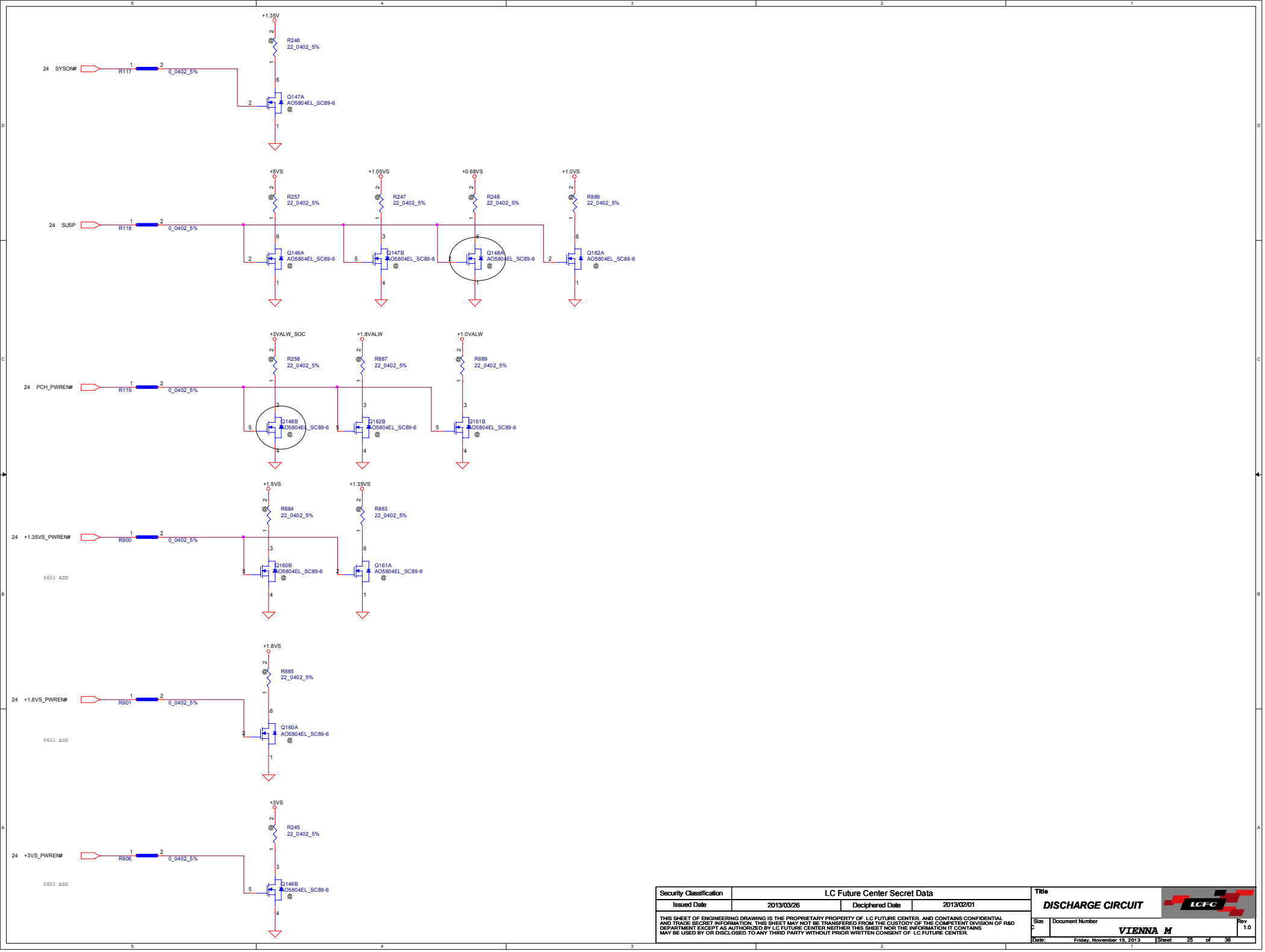

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Issued Date	2013/03/26	Deciphered Date	2013/02/01

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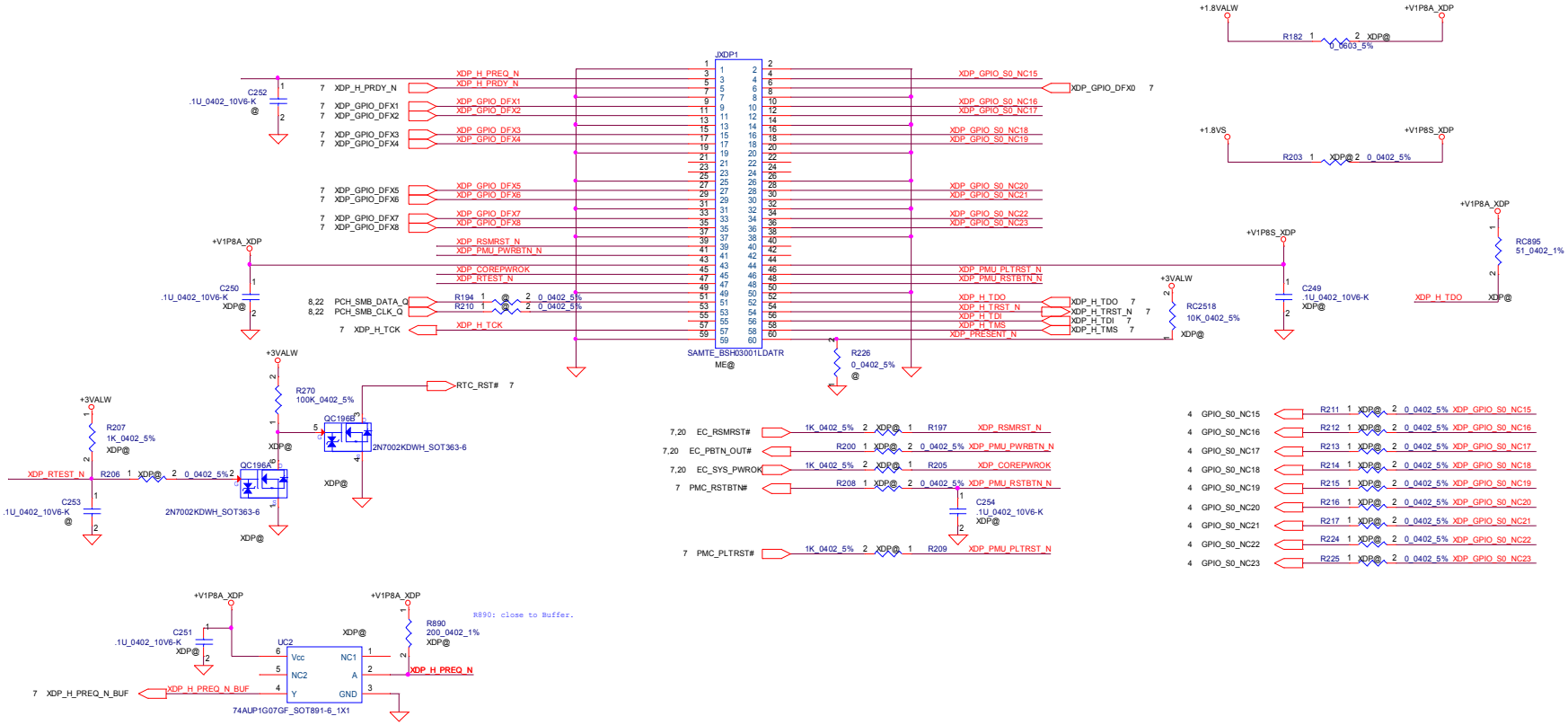
Title: **DISCHARGE CIRCUIT**

Size	Document Number	Rev
C	VIENNA M	1.0

Date: Friday, November 15, 2013 Sheet 25 of 36



FD1 FD2 FD3 FD4 FD5 FD6 0801 DFB需求新增

0531 update Screw

0608 ADD RF SHIELDING

0805 change

pad_c6p0d2p4

H2 H3 H4 H5 H6 H7 HOLEA

pad_c6p0d2p4

pad_c4p0d2p0

H12 H13 HOLEA

pad_c4p0d2p0

PAD_CT6P0

H27 H28 H29 H30 HOLEA 0608

PAD_CT6P0

PAD_SHAPE2P0X4P29

H26 HOLEA

PAD_SHAPE2P0X4P29

pad_shape2p0x4p29

H15 HOLEA

pad_shape2p0x4p29

pad_ct4p0

H22 HOLEA 0608

pad_ct4p0

pad_ct5p0b6p0d3p6

H16 H17 H18 H19 HOLEA

pad_ct5p0b6p0d3p6

pad_shape12p71x6p6d2p4

H23 HOLEA 0613

pad_shape12p71x6p6d2p4

pad_shape21p3x8p07d2p4

H24 HOLEA 0613

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pad_ct6p0b8p0x7p5d2p4

H25 HOLEA 0613

pad_ct6p0b8p0x7p5d2p4

SH5 SH6 SH15 SH16 SH13 SH14 SH18 SH17 ME@

SPRING_FINGER_6.2X1.64

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Issued Date	2013/03/26	Deciphered Date	2013/02/01

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Title	Screw and Hole		
Size	Document Number		Rev
C	VIENNA M		1.0
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Title

HW_Change_List

Size	Document Number	Rev
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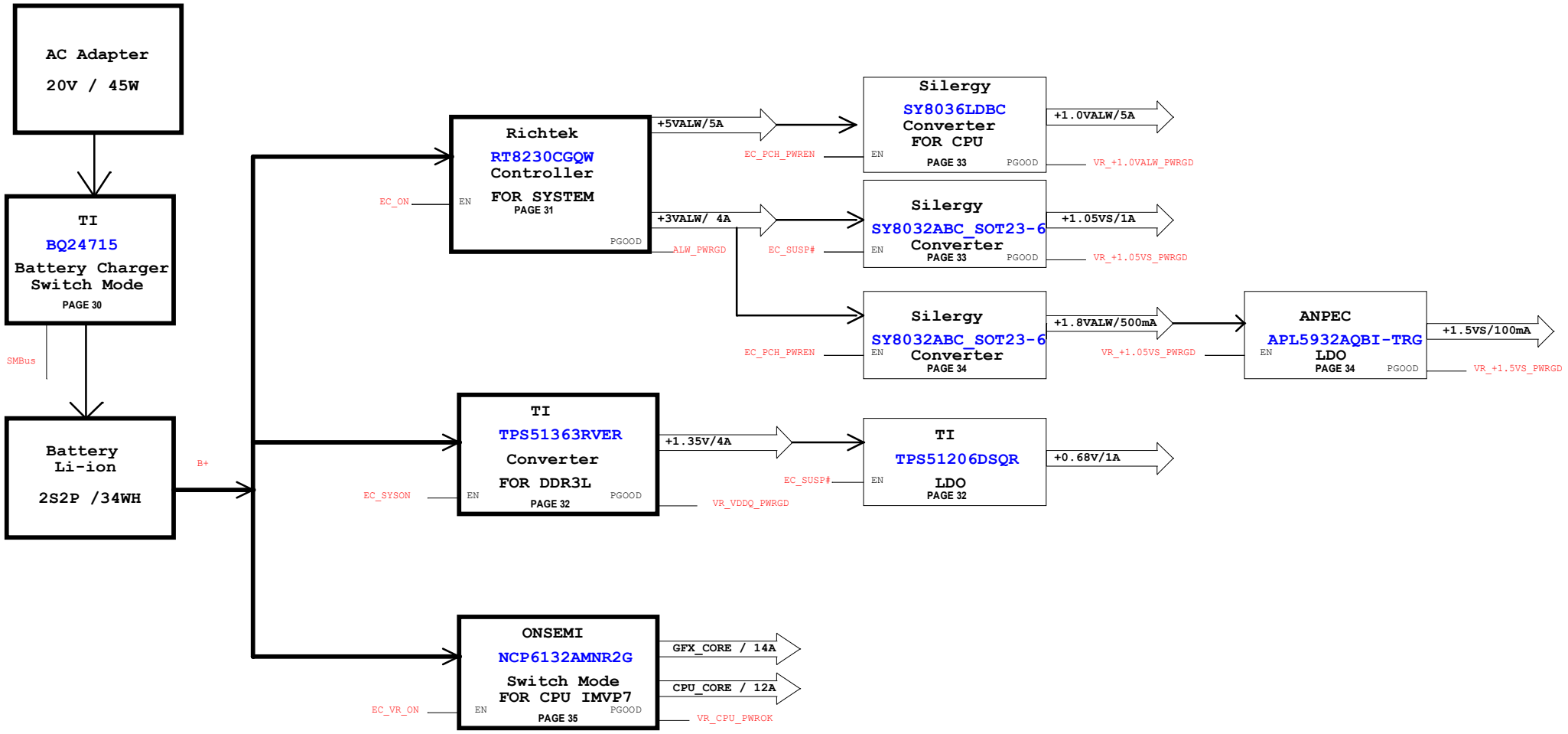

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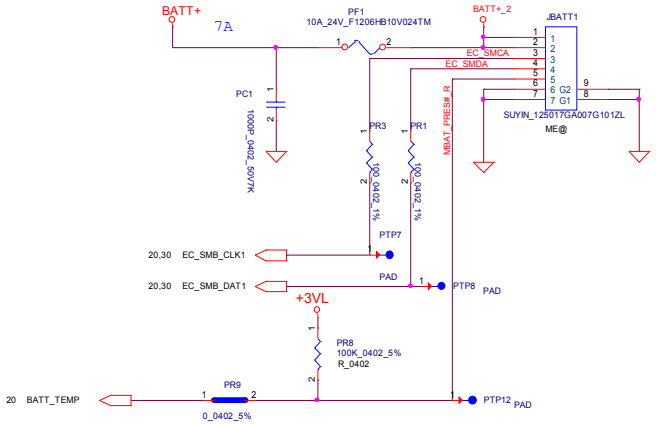
Size: C	Document Number: VIENNA M	Rev: 1.0
Date: Friday, November 15, 2013	Sheet 28 of 36	



Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2013/02/01

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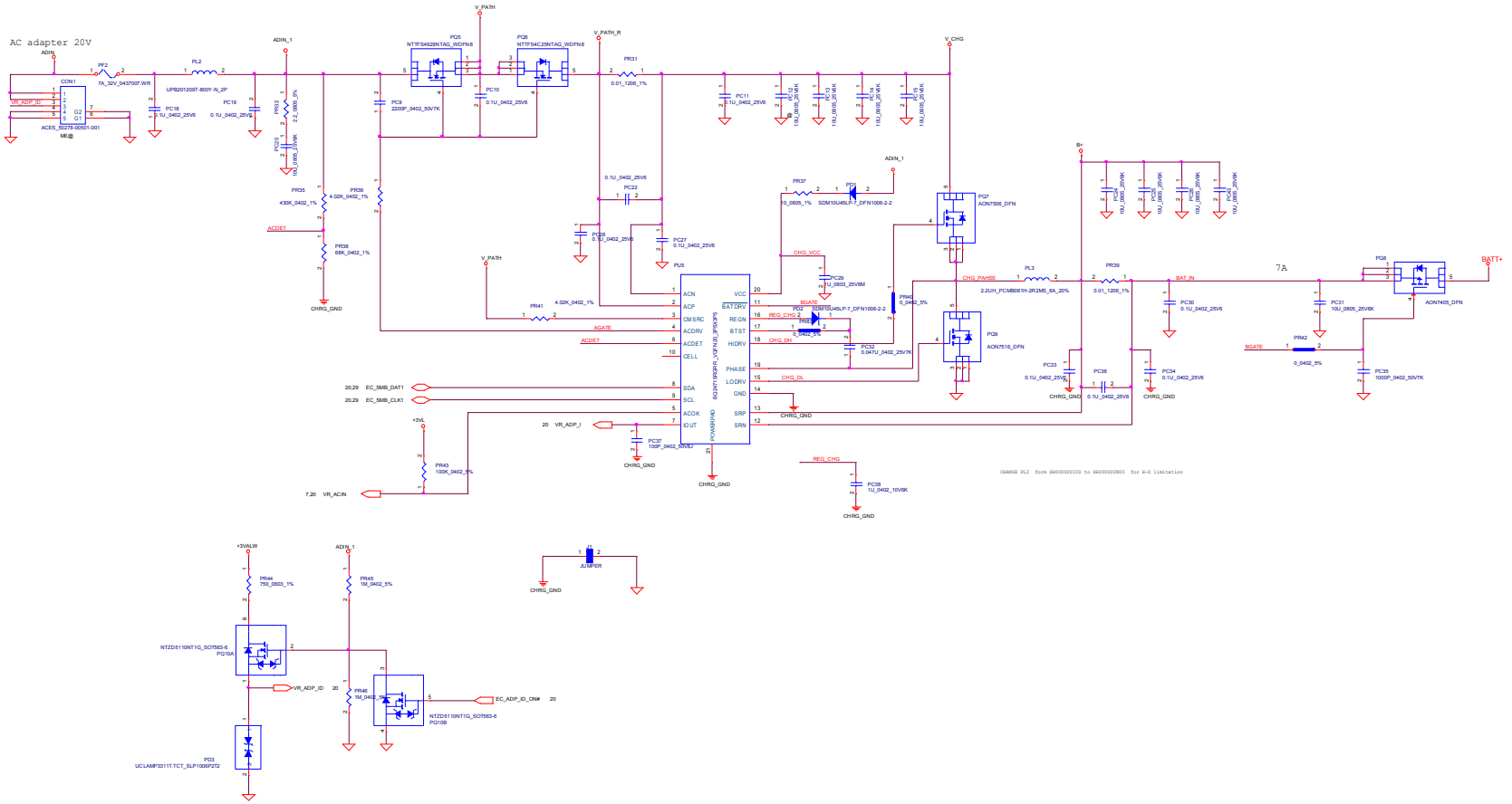
Title: PWR_BATTERY CONN

Size	Document Number	Rev
C	VIENNA M	1.0

Date: Friday, November 15, 2013 Sheet 29 of 36



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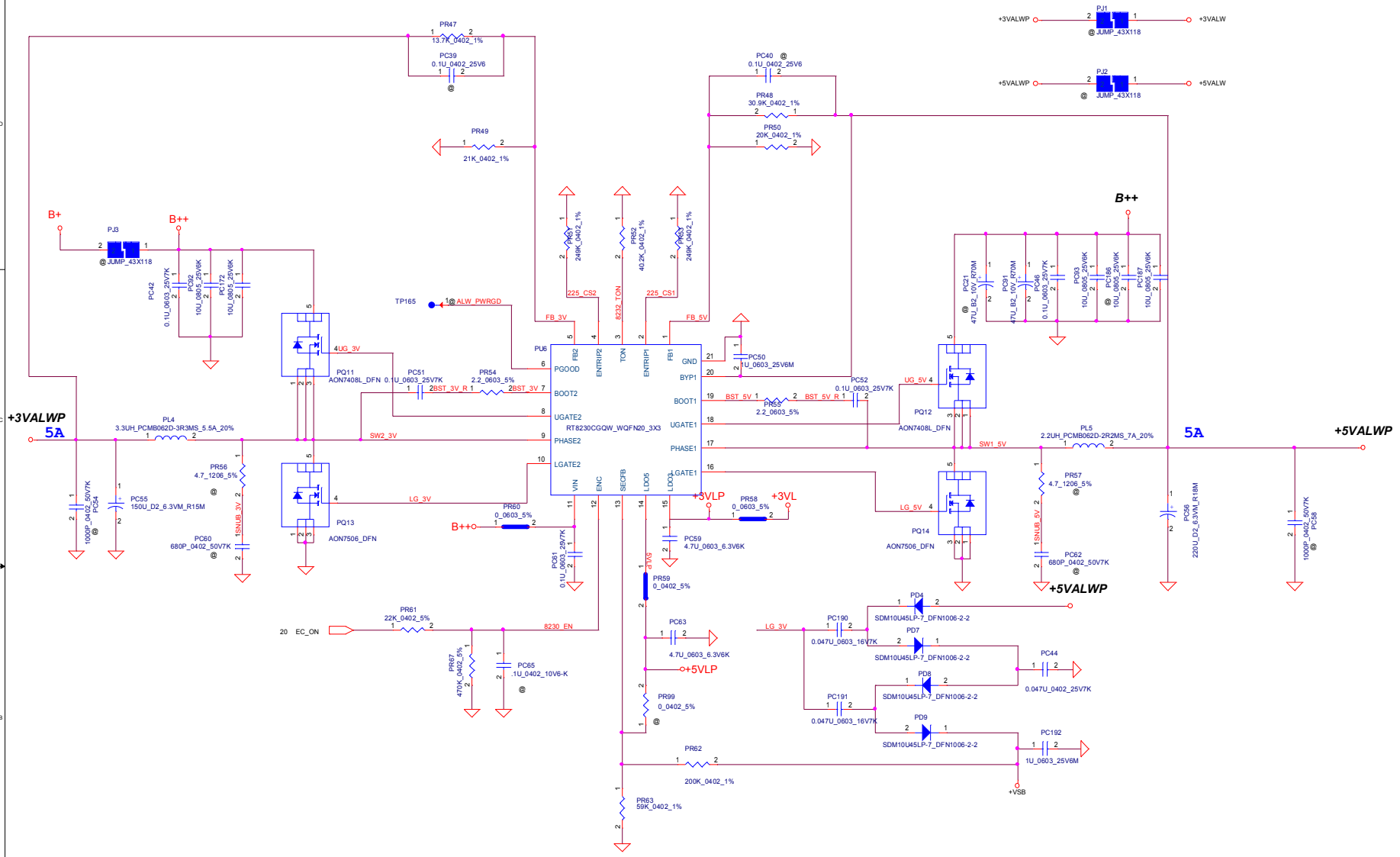
Size	Document Number		Rev
D	VIENNA M		1.0
Date:	Friday, November 15, 2013	Sheet	30 of 36



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Issued Date	2012/12/28	Deciphered Date	2012/12/28

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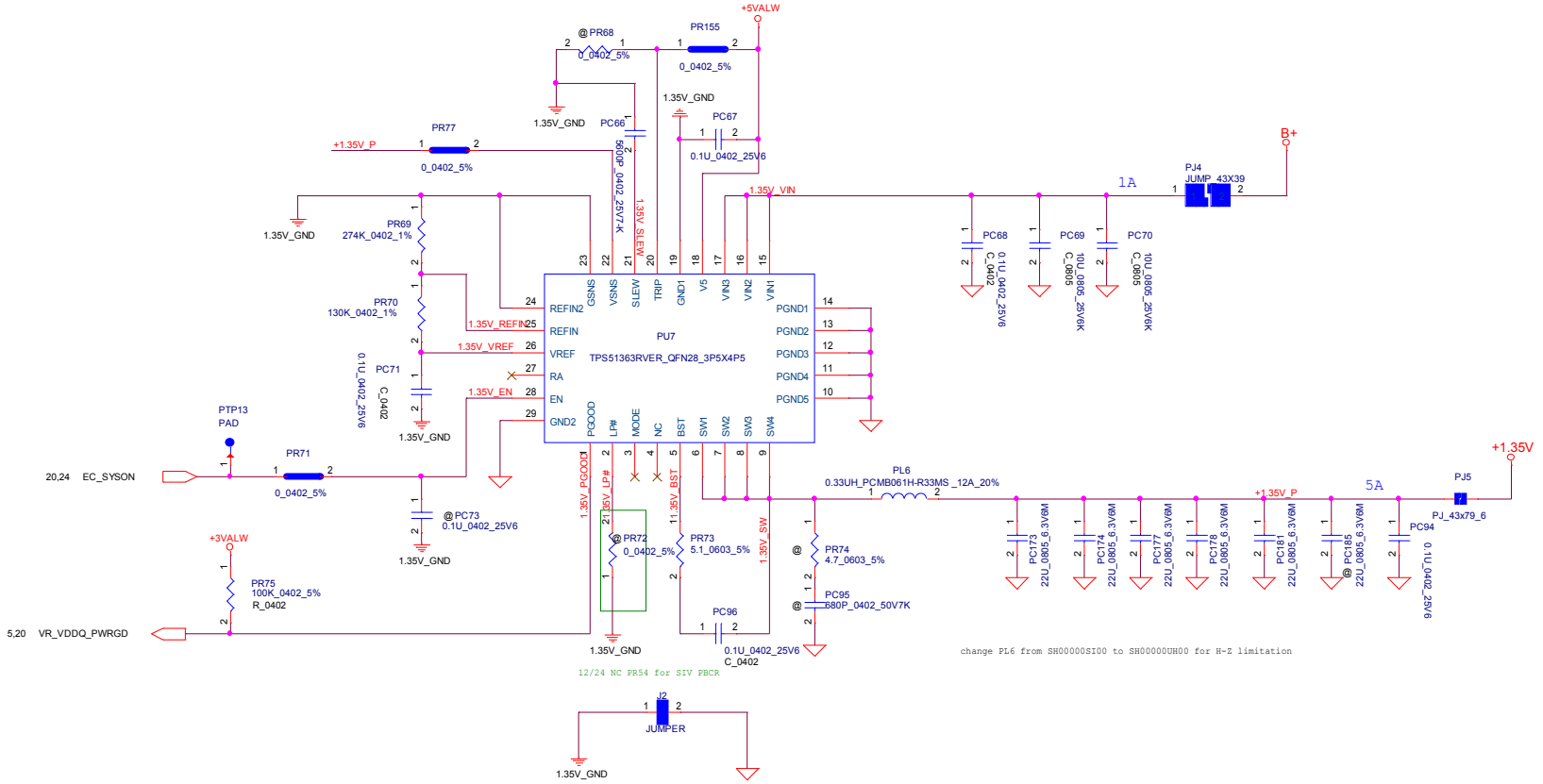
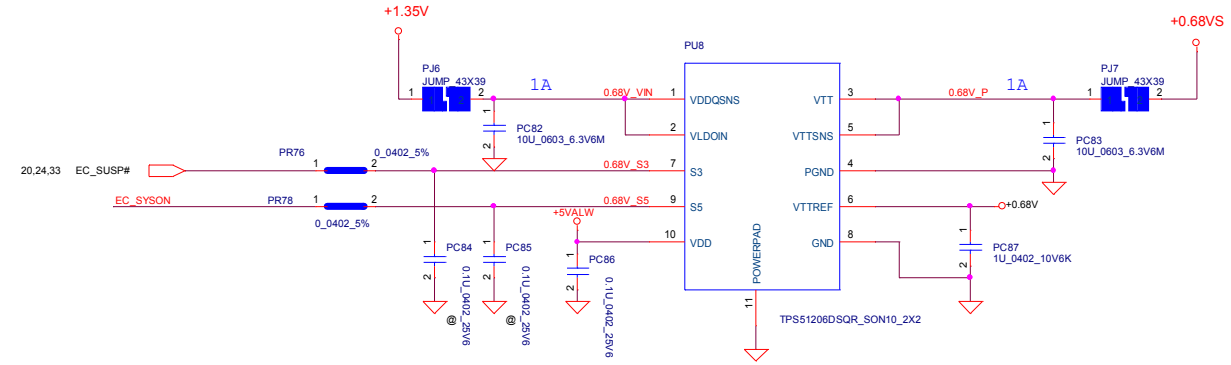
Title	3VALWP/5VALWP		
Size	Document Number		Rev
C	VIENNA M		1.0
Date:	Friday, November 15, 2013	Sheet	31 of 36





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Issued Date	2013/03/26	Deciphered Date	2013/02/01

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Title: PWR_1.35V/0.68VS

Size	Document Number	Rev
Custom	VIENNA M	1.0

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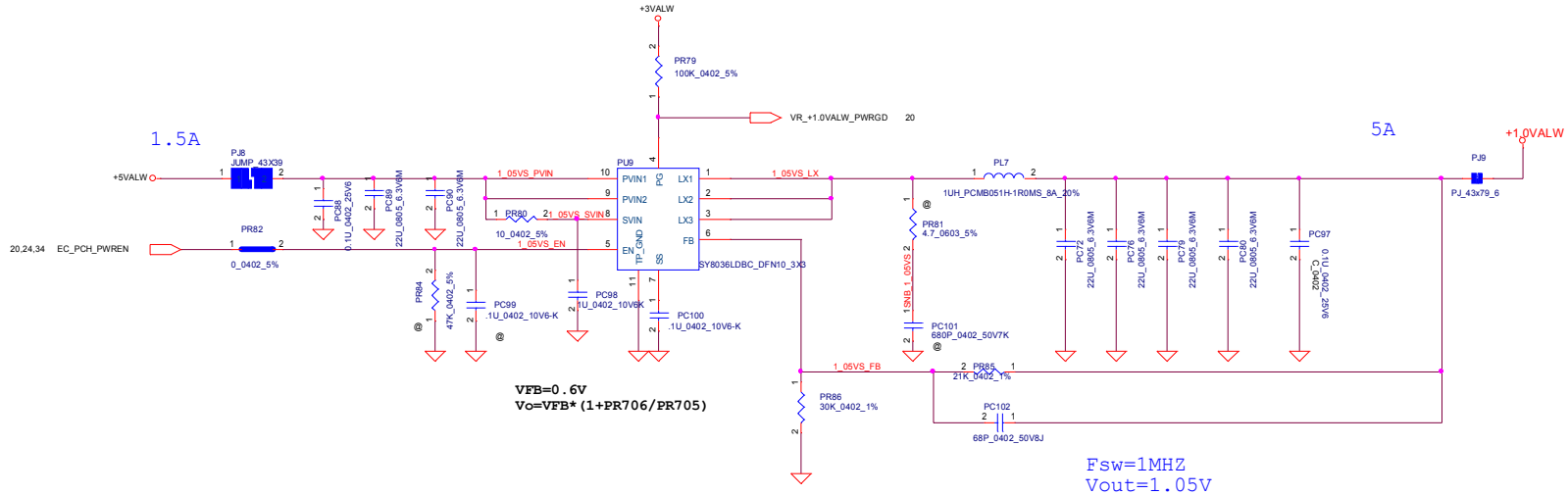

PR92 change from SD03420028J to SD03410038J
PR89 change from to SD03415028J to SD03475028J

Security Classification	LC Future Center Secret Data		
Issued Date	2013/03/26	Deciphered Date	2013/02/01

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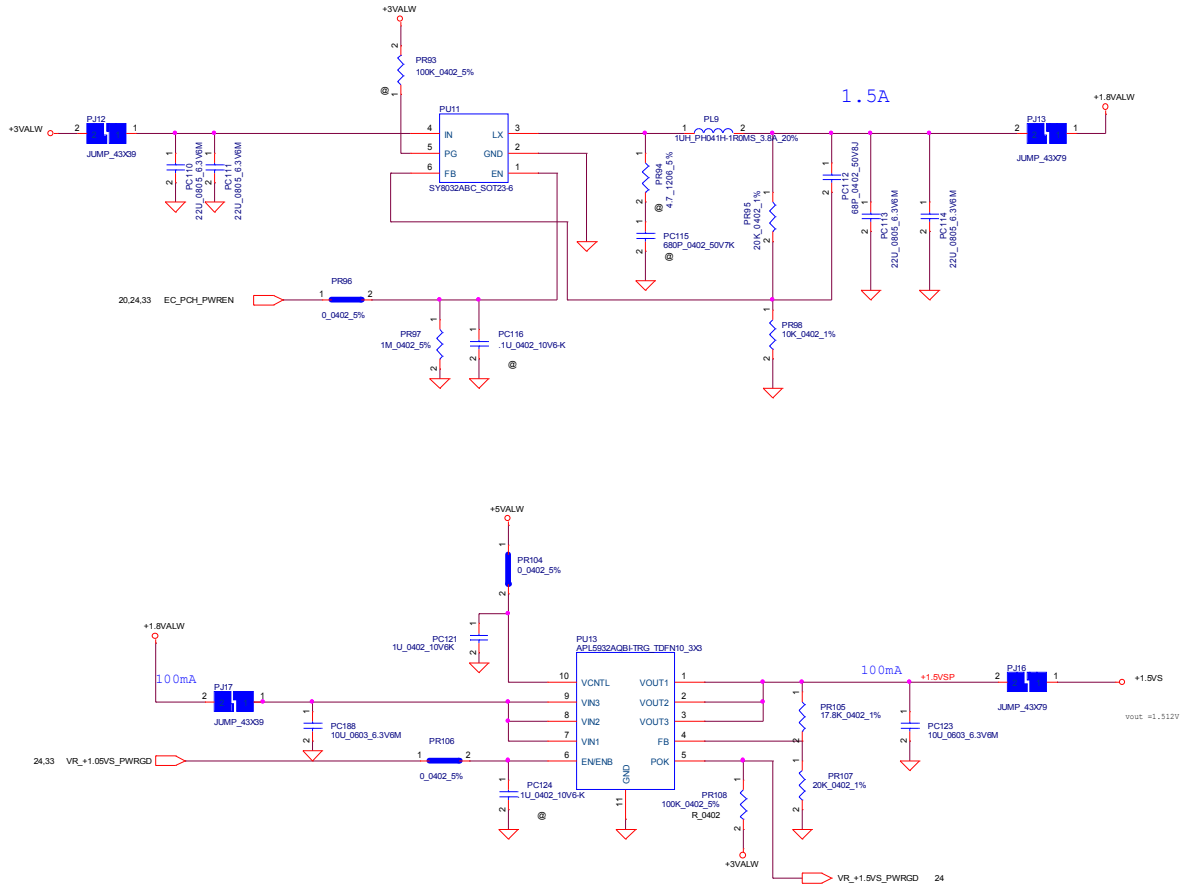
Title: PWR_1.35V/0.68VS

Size	Document Number	Rev
C	VIENNA M	1.0

Date: Friday, November 15, 2013 Sheet 33 of 36



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Issued Date	2013/03/26	Deciphered Date	2013/02/01

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Title: PWR_VCCSA

Size: Custom	Document Number: VIENNA M	Rev: 1.0
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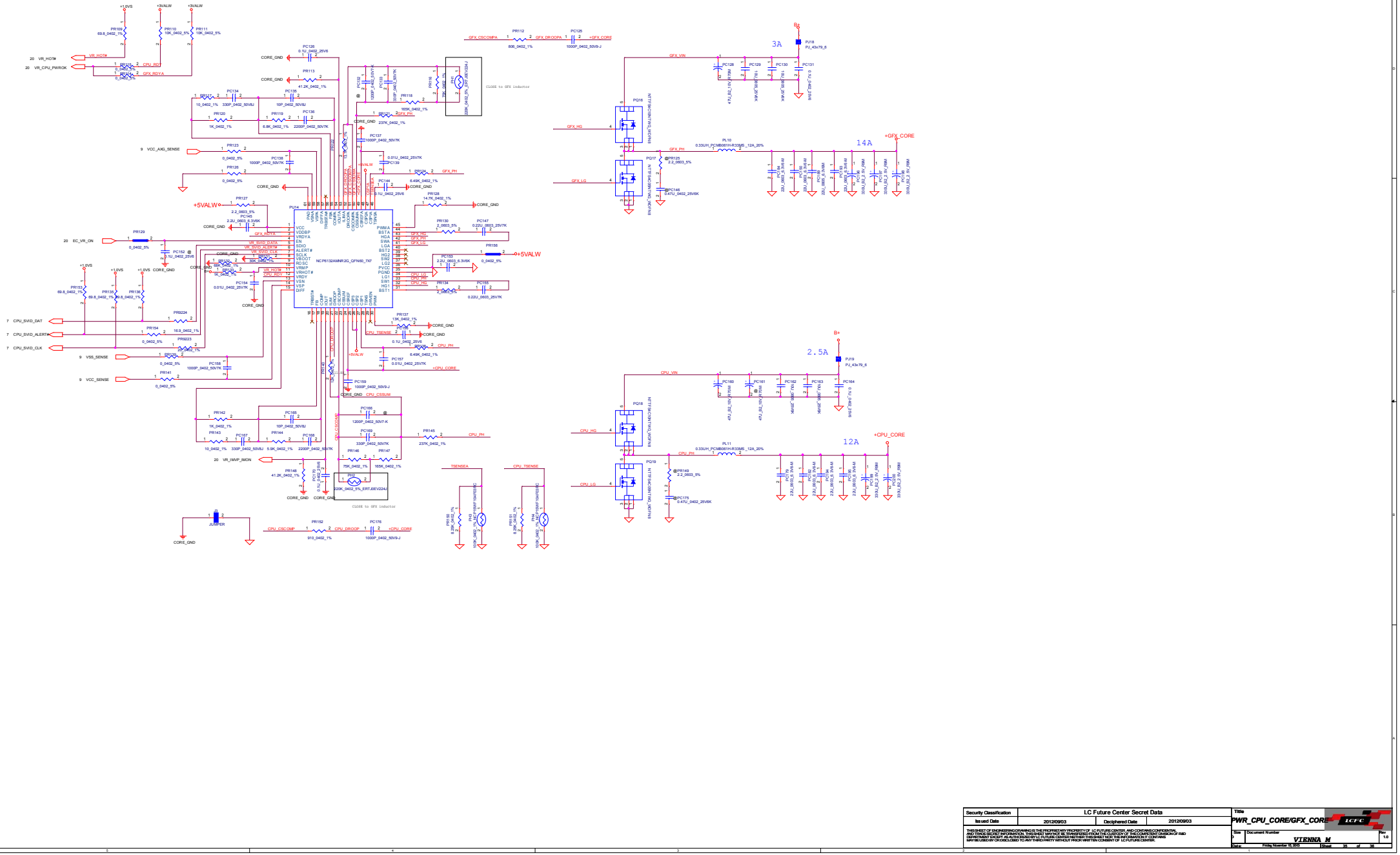

Security Classification	LC Future Center Secret Data		
Issued Date	2012/09/03	Deciphered Date	2012/09/03

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Title: PWR_CPU_CORE/GFX_CORE

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Size	Document Number	Rev
C	***VIENNA M***	1.0

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